DRONACHARYA
College of Engineering

VLSI Design

Subject code:PCCEEE310G

Semester: VI

Unit –I
Basic MOS Transistor

Content

- MOSFET structure
  - Enhancement mode
  - Depletion mode
- Introduction of IC Technology
- IC Fabrication process
  - NMOS Technology
  - PMOS Technology
  - CMOS Technology
  - BICMOS Technology

MOSFET

- Metal oxide semiconductor field transistors can be considered as switch which operates with proper biasing.
- MOSFET is three terminal device source , drain and gate.
- Biasing means application of appropriate voltage at three terminal of MOSET so that it can be moved from on to off state or vice versa.

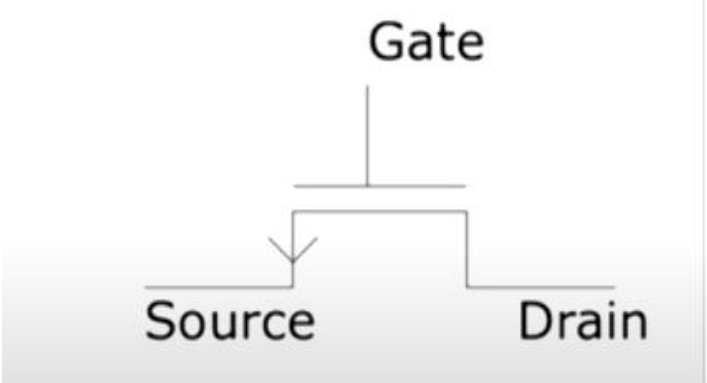


Figure : MOS device Schematic

MOSFET

- Metal-Oxide-Semiconductor (MOS) structure is created by superimposing several layers of conducting and insulating materials to form a sandwich- like structure.
- These structures are manufactured using a series of chemical processing steps involving oxidation of the silicon, selective introduction of dopants, and deposition and etching of metal wires and contacts.
- Transistor operation is controlled by electric fields so the devices are also called Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)
- Types of MOSFET

✓ Based on material properties

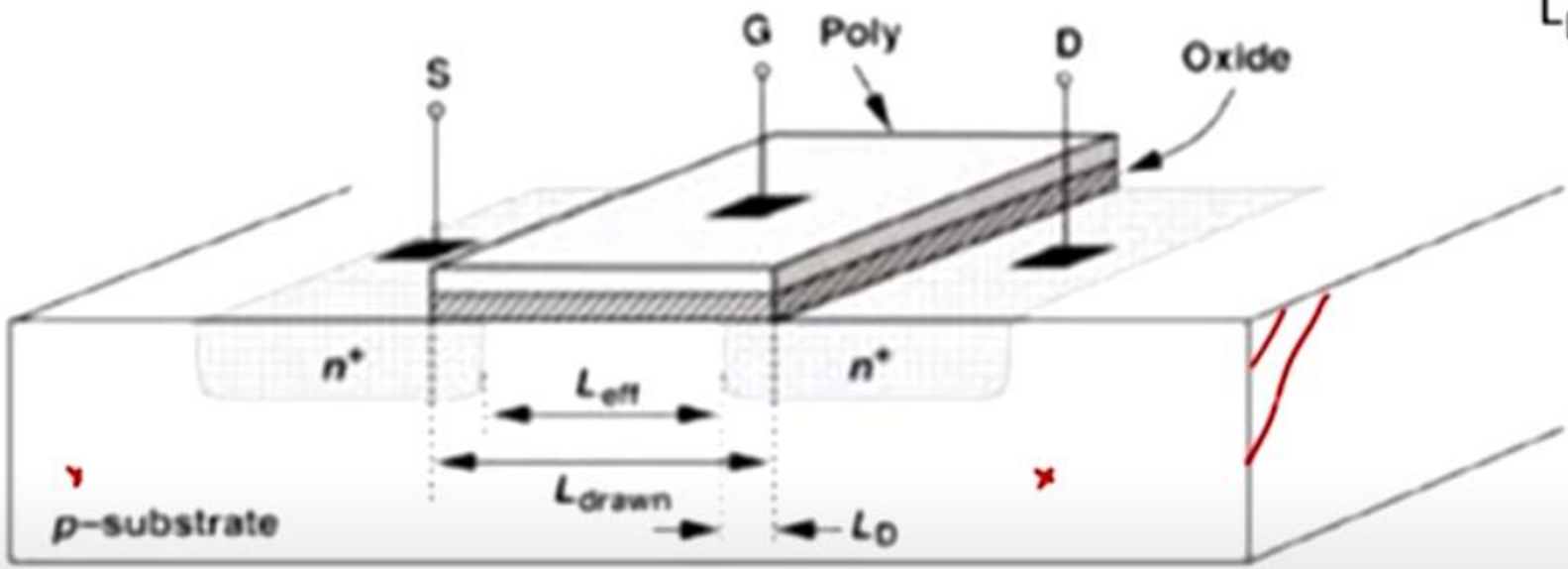
- N Mos- where electrons are charge carriers
- P Mos- where holes are charge carriers

MOSFET

✓Based on electrical properties

- Enhancement mode MOSFET
- Depletion mode MOSFET
- So technically four types of MOSFET
  - N channel Enhancement mode MOSFET
  - P channel Enhancement mode MOSFET
  - P channel Depletion mode MOSFET
  - N channel Depletion mode MOSFET

MOSFET Structure



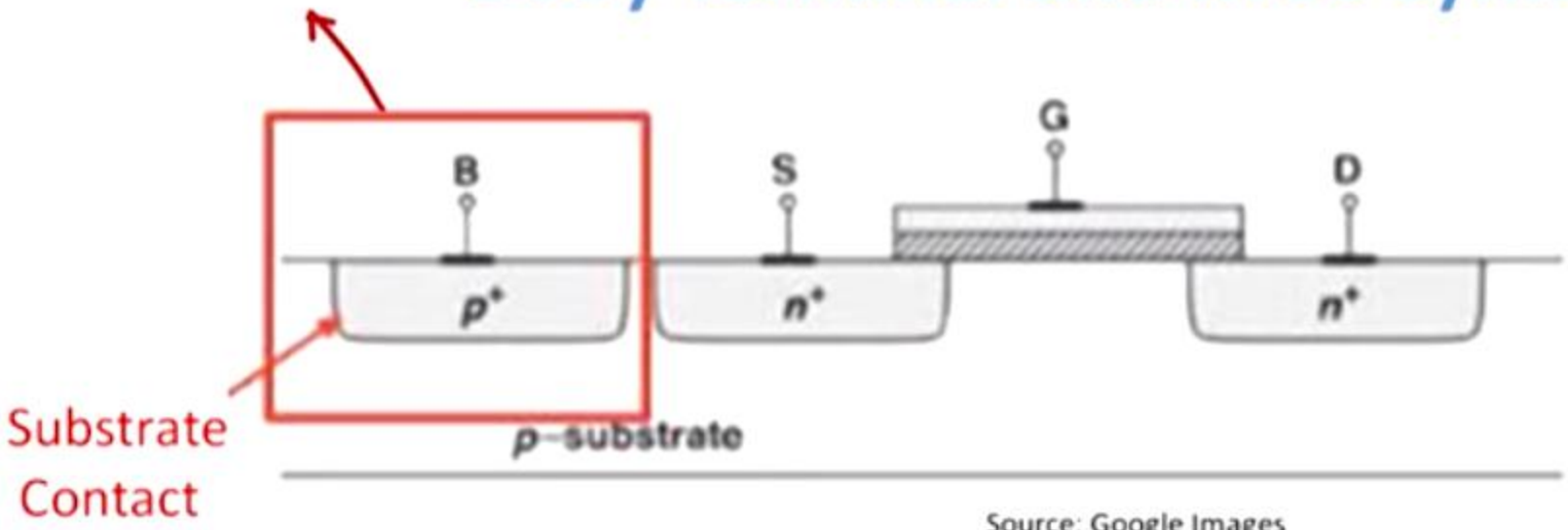
L_D: Side Diffusion Length

$L_{eff} = L_{drawn} - 2L_D$

Introduction

- Each transistor consists of a stack of the conducting gate, an insulating layer of silicon dioxide (SiO2), and the silicon wafer, also called the substrate, or body, or bulk.
- An nMOS transistor is built with a p-type body and has regions of n-type
  - semiconductor adjacent to the gate called the source and drain
- A pMOS consists of p-type source and drain regions with an n-type body.

Body Terminal and MOS symbols



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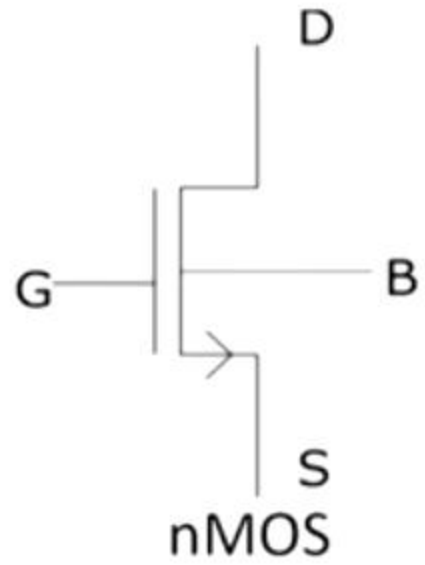
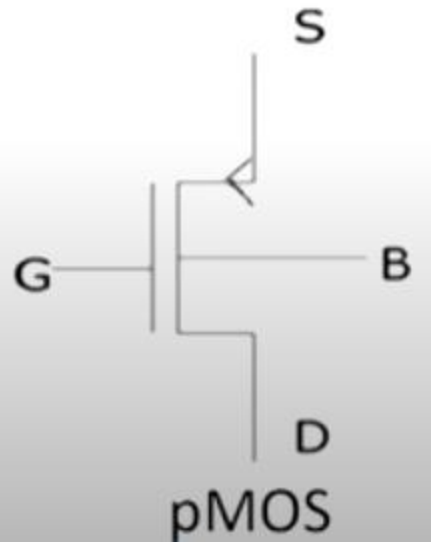
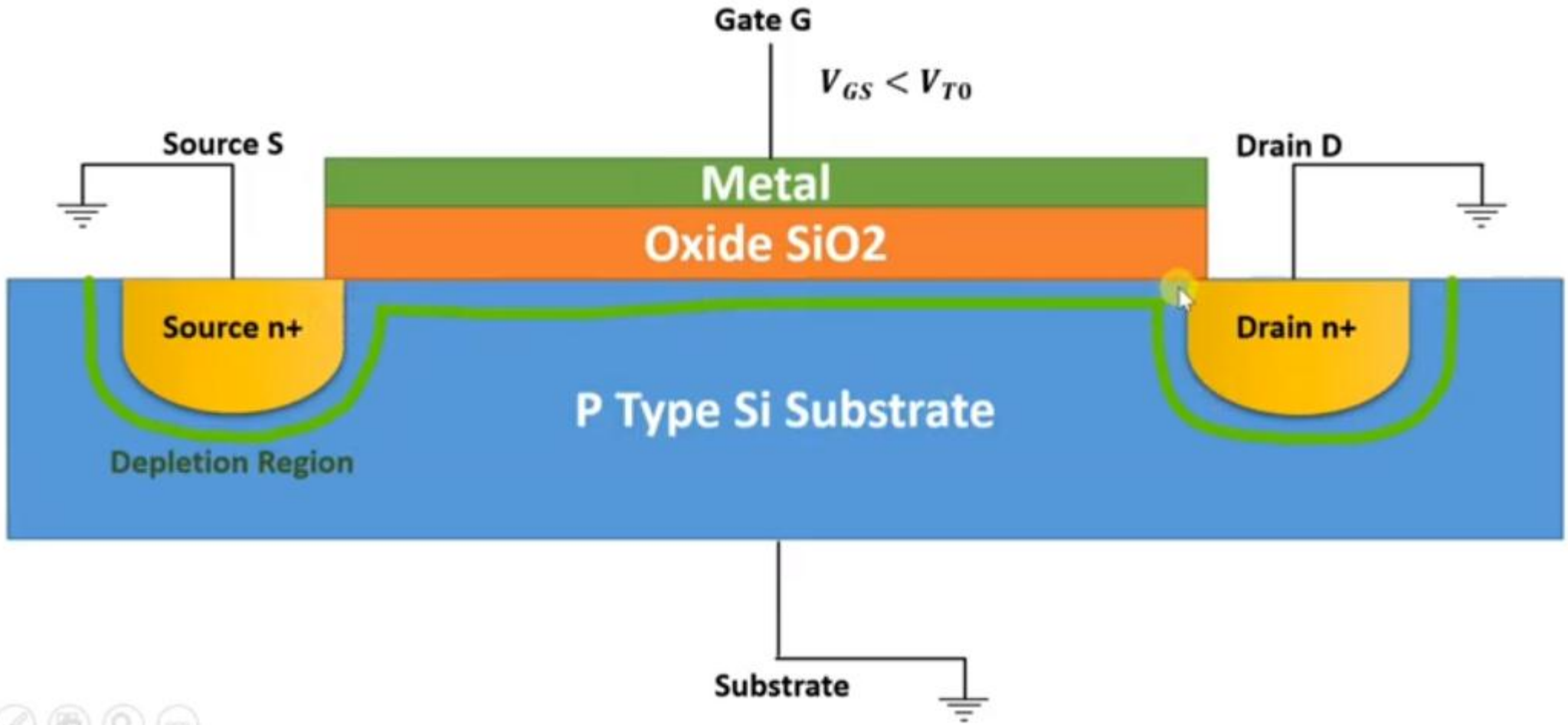




- The substrate bias should be connected with the negative most supply of the system.
- nMOS and pMOS are in general made in same wafer, in which one device can placed in local substrate called as well.

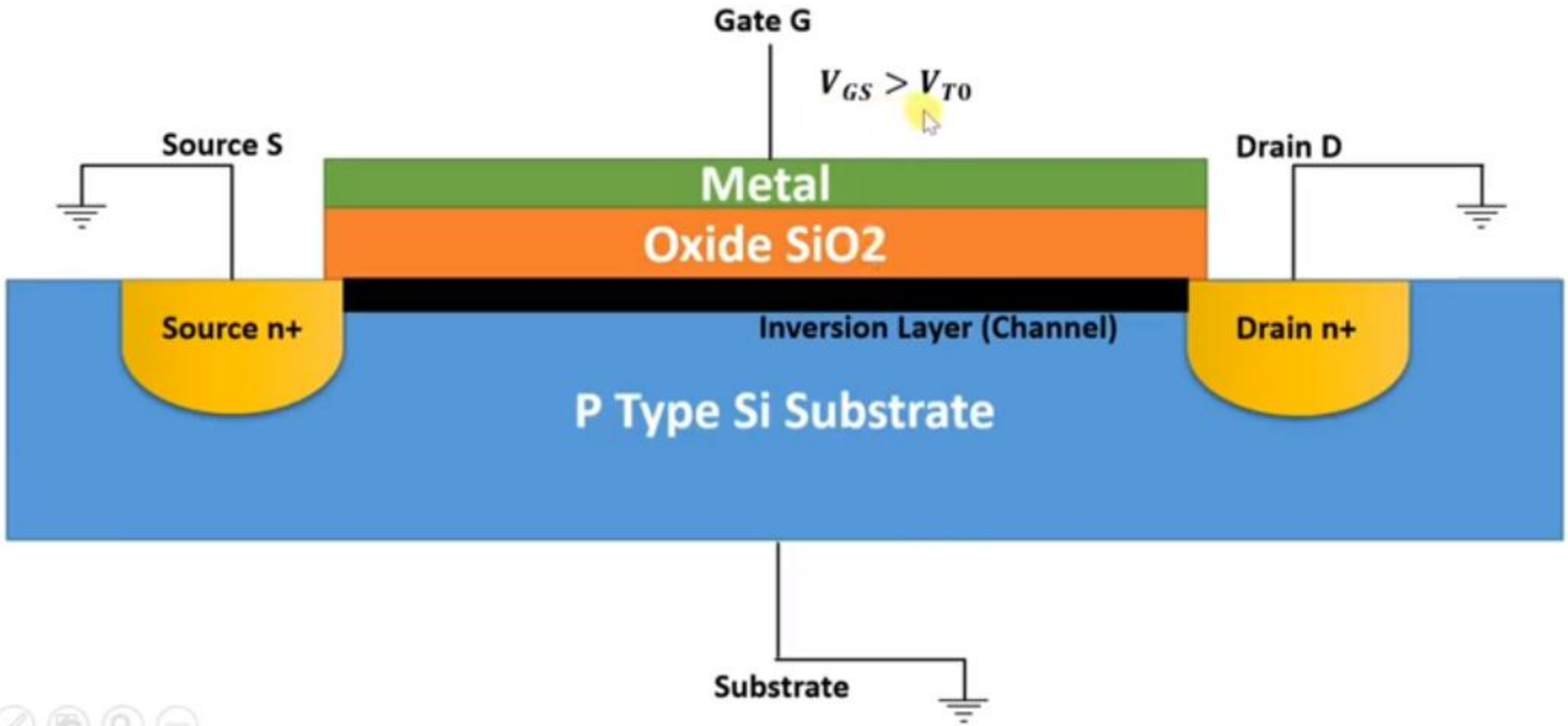
Working of n Channel MOSFET in cut off region



MOSFET :Cutoff Region mode

- When $V_{GS} < V_T$, there is no channel formed between the Drain and Source and hence I_{DS}=0 A
- This region is called the *Cutoff Region*
- *T*his region of operation is when the Transistor is OFF

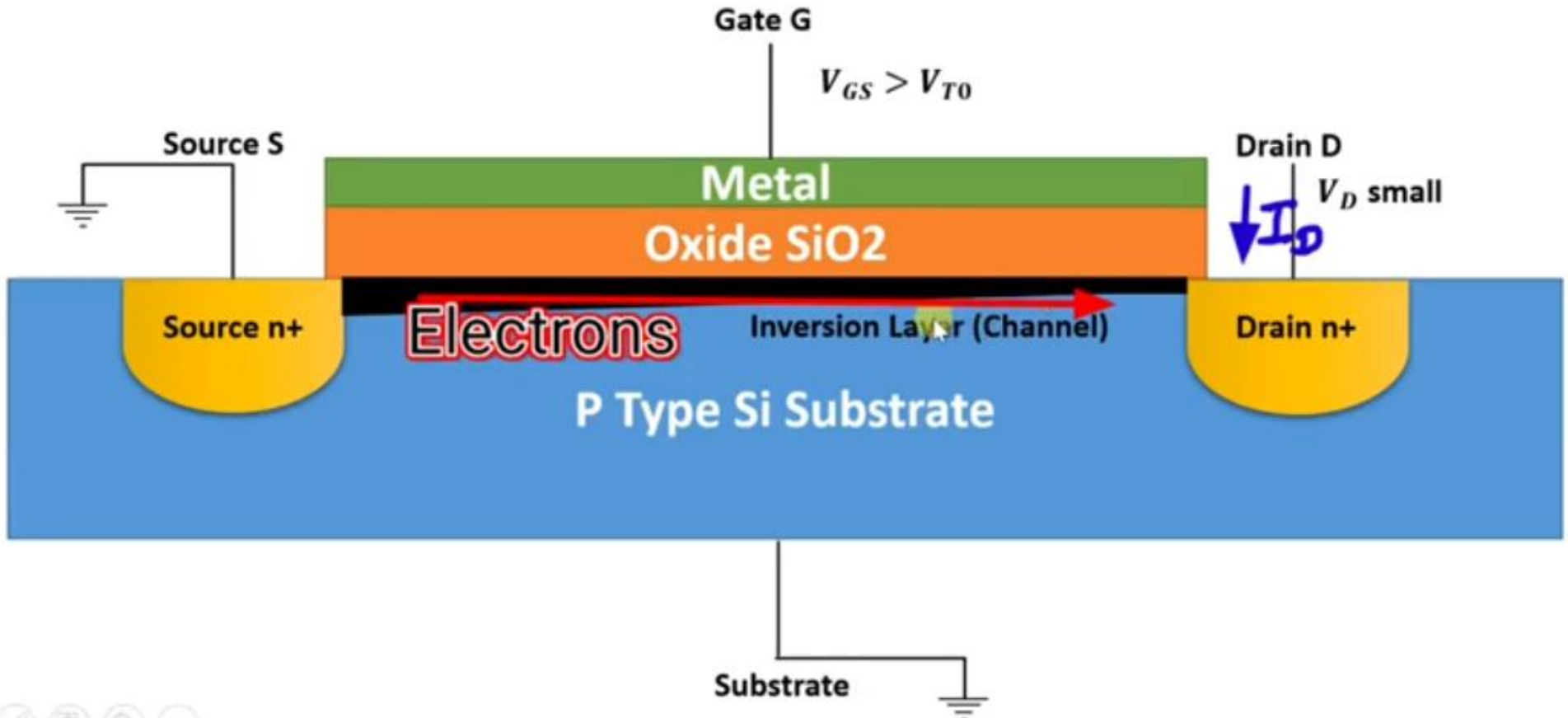
Working of n Channel MOSFET cut off region



MOSFET : Cutoff Region mode

- When VGS > VT, a channel is formed. IDS is dependent on the VDS voltage
- When VDS = 0v, no current flows.

Working of n Channel MOSFET in Linear region



MOSFET: Linear Region mode

• If VGS > VT and VDS > 0, then a current will flow from the Drain to Source (IDS).The MOSFET operates like a voltage controlled resistor which yields a *linear* relationship between the applied voltage (VDS) and the resulting current (IDS)

• For this reason, this mode of operation is called the *Linear Region. T*his region is also sometimes called the *triode region* (we'll use the term "linear")

• VDS can increase up to a point where the current ceases to increase linearly (saturation)

• We denote the highest voltage that VDS can reach and still yield a linear increase in current as the *saturation voltage* or VDSAT

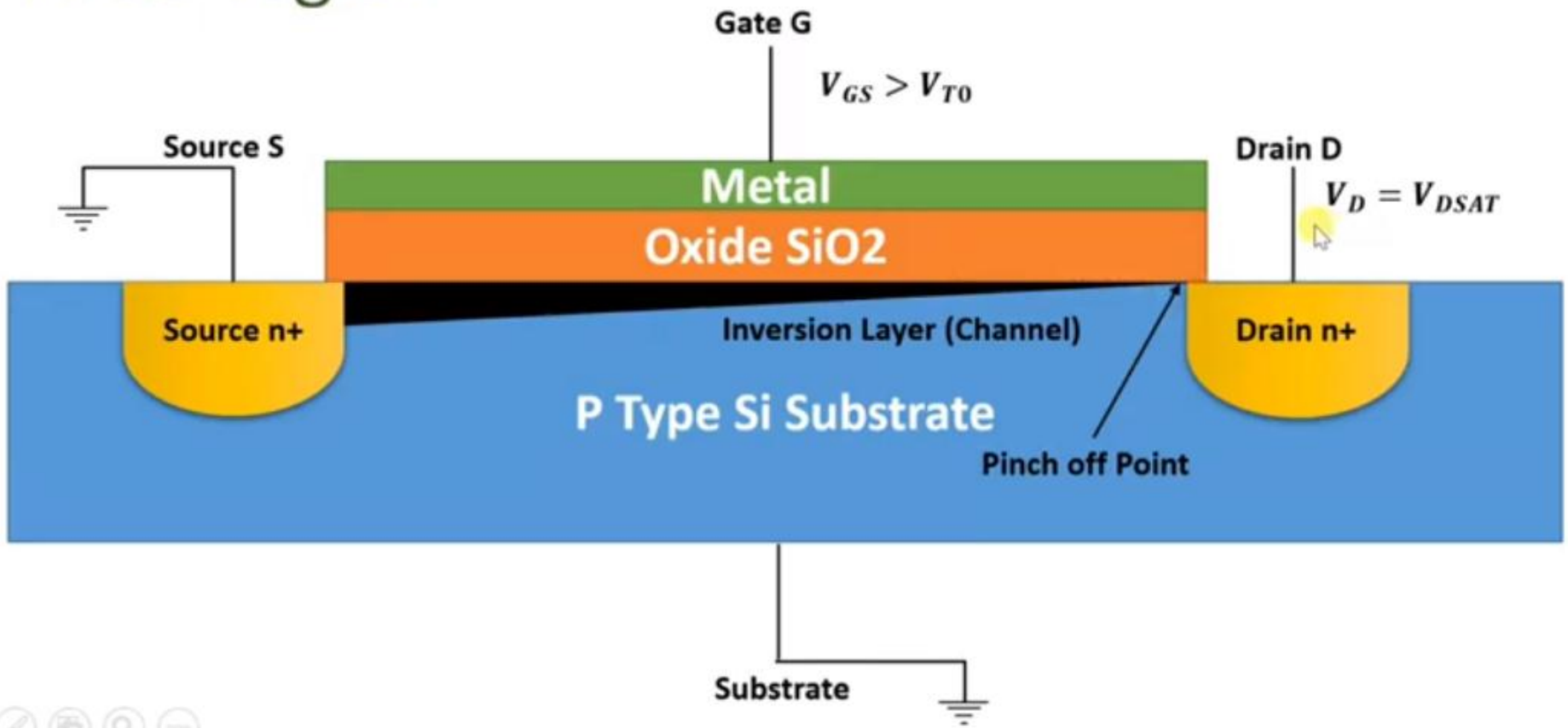
when a voltage is applied at VD, its positive charge pushes the majority charge carriers (holes) that exist at the edge of the depletion region further from the Drain.

- As the depletion region increases, it becomes more difficult for the Gate voltage to induce an inversion layer. This results in the inversion layer depth decreasing near the drain.
- As VD increases further, it eventually causes the inversion layer to be *pinched-off* and prevents the current flow to increase any further.
- This point is defined as the *saturation voltage* (VDSAT)
- From this, we can define the *linear region* as:

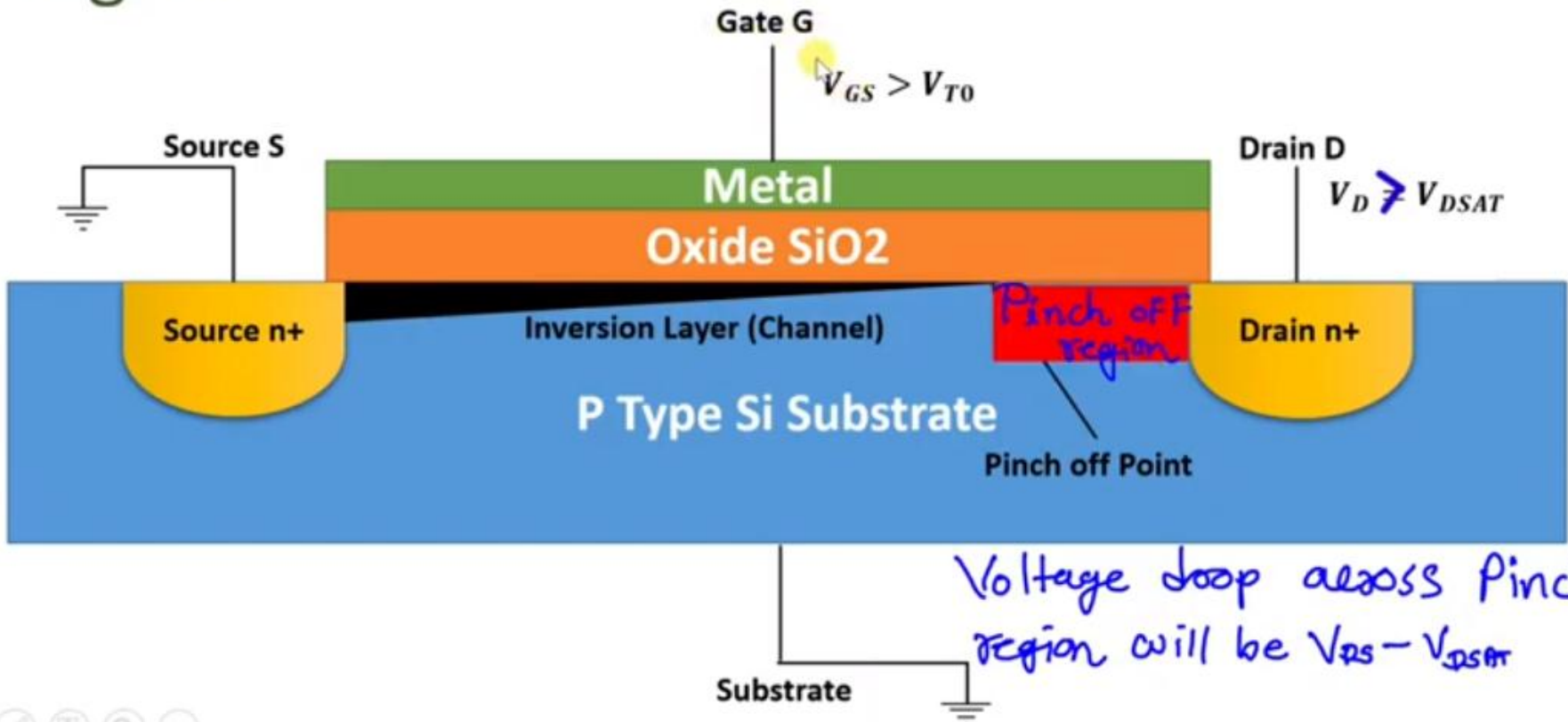
$$VGS > VT$$

$$0 < VDS < VDSAT$$

Working of n Channel MOSFET threshold of linear region



Working of n Channel MOSFET in saturation region



Voltage drop across Pinch off region will be $V_{DS} - V_{DSAT}$

MOSFET : Saturation Region mode

- MOSFET is defined as being in saturation when: Saturation Region :

$$VGS > VT \text{ and } VDS > (VGS-VT)$$

- An increase in VDS does not increase IDS because the channel is *pinched-off*
- However, an increase in VGS DOES increase IDS by increasing the channel depth and hence the amount of current that can be conducted.

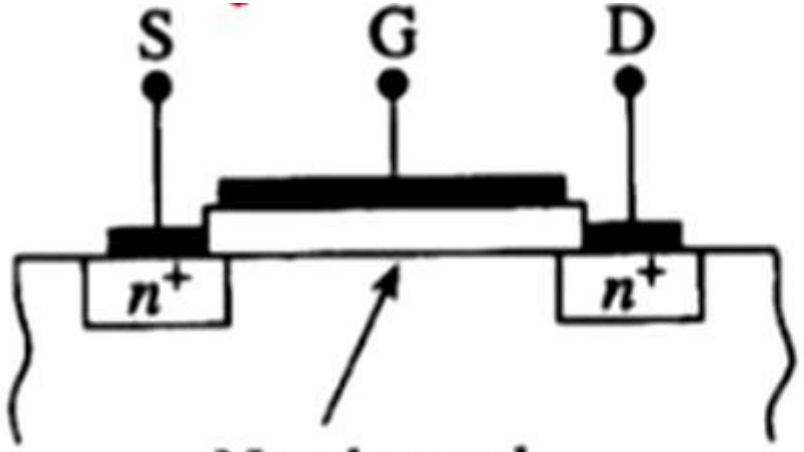
MOSFET Regions of Operation

- Cut-Off Region
  When VGS < VT, no conductive channel is present and IDS = 0, the cutoff region.
- Ohmic or Linear Region

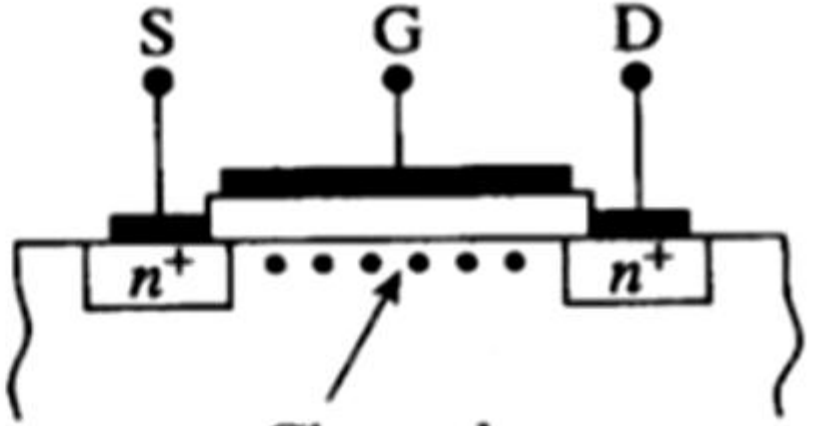
  Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.
- Saturation Region

  In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

Types of MOSFET



No channel
when $V_G = 0$
Enhancement MOSFET



Channel
when $V_G = 0$
Depletion MOSFET

Enhancement-mode MOSFET

- For the **n-channel enhancement MOS transistor** a drain current will only flow when a gate voltage (VGS) is applied to the gate terminal greater than the threshold voltage (VTH) level in which conductance takes place making it a transconductance device.
- The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.
- Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, ID through the channel. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor “ON”, while a zero or -VGS turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

Enhancement-mode MOSFET

- The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor “OFF”, while -VGS turns the transistor “ON”.

n-channel Enhancement-type MOSFET

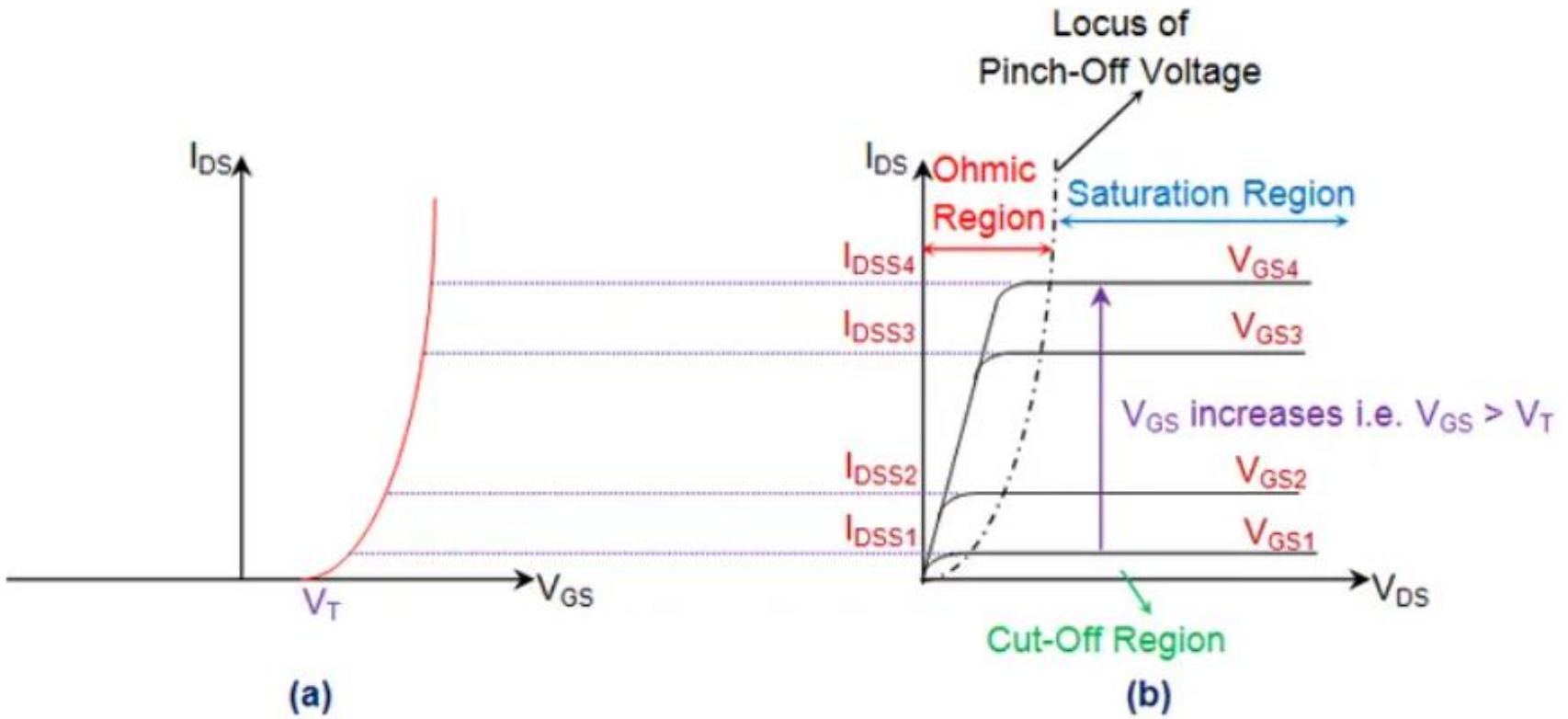


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Transfer characteristics

- The transfer characteristics (drain-to-source current I_{DS} versus gate-to-source voltage V_{GS}) of **n-channel Enhancement-type MOSFETs**. From this, it is evident that the current through the device will be zero until the V_{GS} exceeds the value of threshold voltage V_T. This is because under this state, the device will be void of channel which will be connecting the drain and the source terminals. Under this condition, even an increase in V_{DS} will result in no current flow as indicated by the corresponding output characteristics (I_{DS} versus V_{DS}) shown by Figure 1b. As a result this state represents nothing but the cut-off region of MOSFET's operation.
- Next, once V_{GS} crosses V_T, the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the V_{GS} (saturation region of operation) i.e. as V_{GS} increases, even the saturation current flowing through the device also increases. This is evident by Figure 1b where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, I_{DSS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on and so forth. Further, Figure 1b also shows the locus of pinch-off voltage (black discontinuous curve), from which V_P is seen to increase with an increase in $V_{GS.}$

p-channel Enhancement-type MOSFET

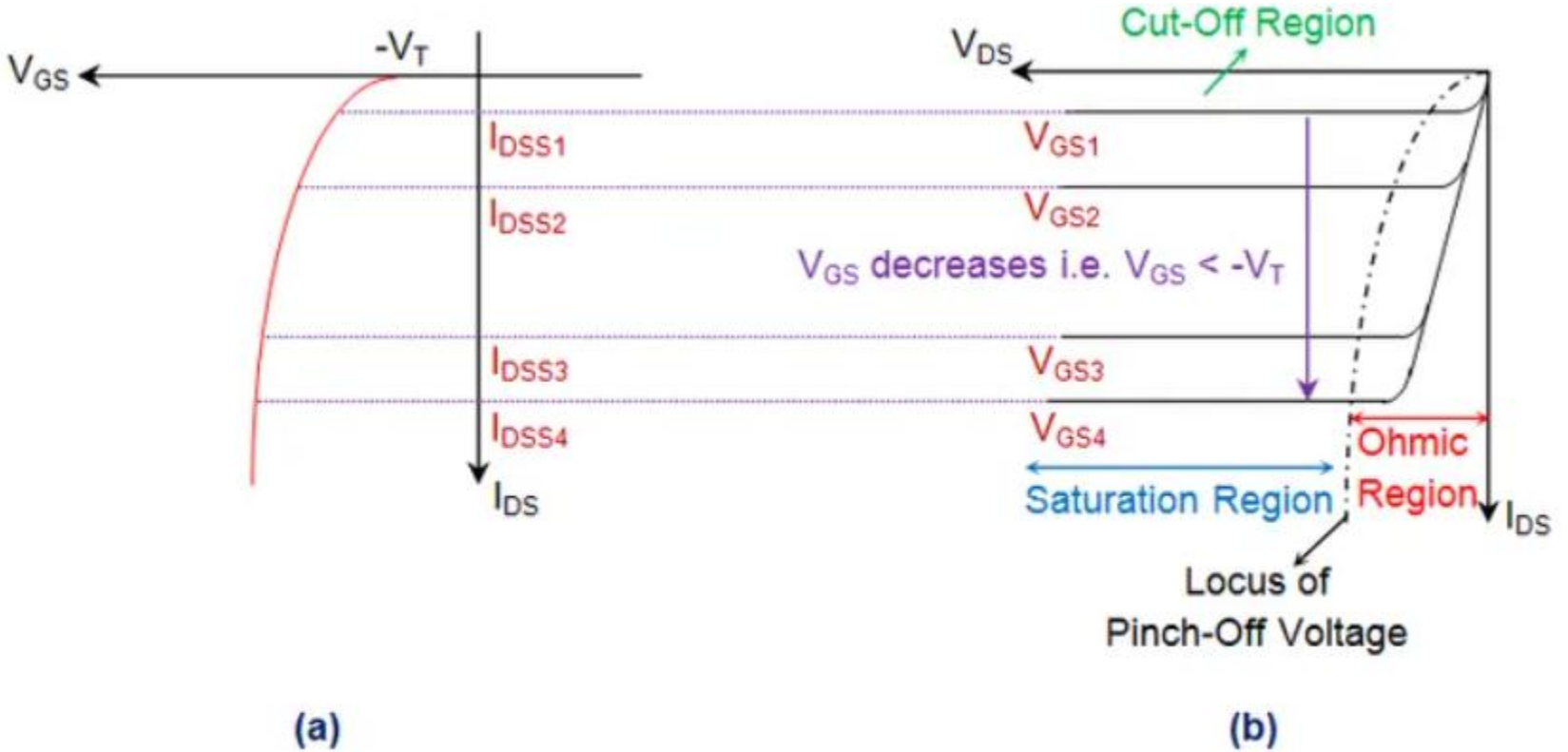


Figure 2 *p*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Transfer characteristics

- Figure 2a shows the transfer characteristics of p-type enhancement MOSFETs from which it is evident that IDS remains zero (cutoff state) until VGS becomes equal to -VT. This is because, only then the channel will be formed to connect the drain terminal of the device with its source terminal. After this, the IDS is seen to increase in reverse direction (meaning an increase in ISD, signifying an increase in the device current which will flow from source to drain) with the decrease in the value of VDS. This means that the device is functioning in its ohmic region wherein the current through the device increases with an increase in the applied voltage (which will be VSD).
- However as VDS becomes equal to –VP, the device enters into saturation during which a saturated amount of current (IDSS) flows through the device, as decided by the value of VGS. Further it is to be noted that the value of saturation current flowing through the device is seen to increase as the VGS becomes more and more negative i.e. saturation current for VGS3 is greater than that for VGS2 and that in the case of VGS4 is much greater than both of them as VGS3 is more negative than VGS2 while VGS4 is much more negative when compared to either of them (Figure 2b). In addition, from the locus of the pinch-off voltage it is also clear that as VGS becomes more and more negative, even the negativity of VP also increases.

Depletion -mode MOSFET

The **Depletion-mode MOSFET**, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$ making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, $+V_{GS}$ will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. While a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

n-channel Depletion-type MOSFET

- The transfer characteristics of **n-channel depletion MOSFET** shown by Figure 3a indicate that the device has a current flowing through it even when V_{GS} is 0V. This indicates that these devices conduct even when the gate terminal is left unbiased, which is further emphasized by the V_{GS0} curve of Figure 3b. Under this condition, the current through the MOSFET is seen to increase with an increase in the value of V_{DS} (Ohmic region) untill V_{DS} becomes equal to pinch-off voltage V_P. After this, I_{DS} will get saturated to a particular level I_{DSS} (saturation region of operation) which increases with an increase in V_{GS} i.e. $I_{DSS3} > I_{DSS2} > I_{DSS1}$, as $V_{GS3} > V_{GS2} > V_{GS1}$. Further, the locus of the pinch-off voltage also shows that V_P increases with an increase in V_{GS}.

n-channel Depletion-type MOSFET

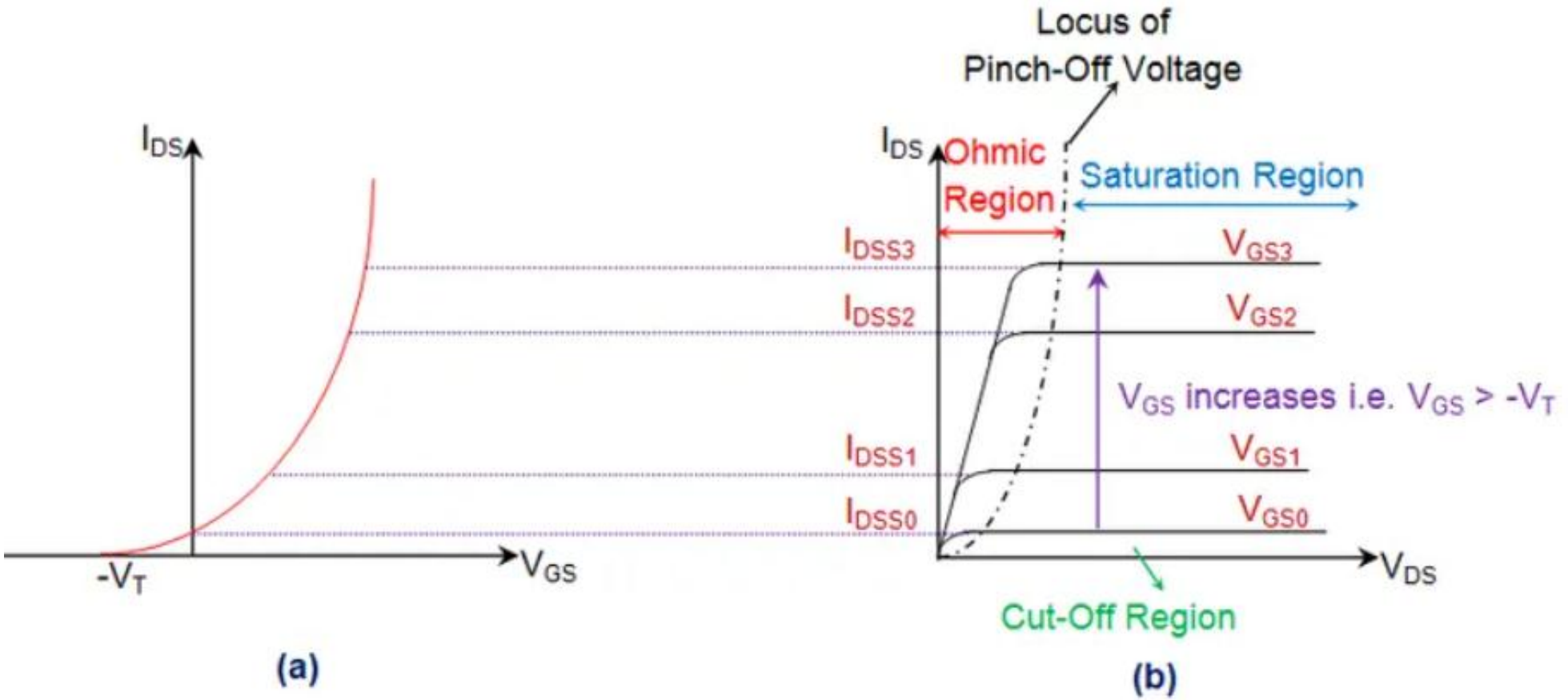


Figure 3 *n*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

p-channel Depletion-type MOSFET

- The transfer characteristics of p-channel depletion mode MOSFETs (Figure 4a) show that these devices will be normally ON, and thus conduct even in the absence of VGS. This is because they are characterized by the presence of a channel in their default state due to which they have non-zero IDS for VGS = 0V, as indicated by the VGS0 curve of Figure 4b. Although the value of such a current increases with an increase in VDS initially (ohmic region of operation), it is seen to saturate once the VDS exceeds VP (saturation region of operation). The value of this saturation current is determined by the VGS, and is seen to increase in negative direction as VGS becomes more and more negative. For example, the saturation current for VGS3 is greater than that for VGS2 which is however greater when compared to that for VGS1. This is because VGS2 is more negative when compared to VGS1, and VGS3 is much more negative when compared to either of them. Next, one can also note from the locus of pinch-off point that even VP starts to become more and more negative as the negativity associated with the VGS increases.
  Lastly, it is evident from Figure 4a that inorder to switch these devices OFF, one needs to increase VGS such that it becomes equal to or greater than that of the threshold voltage VT. This is because, when done so, these devices will be deprived of their p-type channel, which further drives the MOSFETs into their cut-off region of operation.

p-channel Depletion-type MOSFET

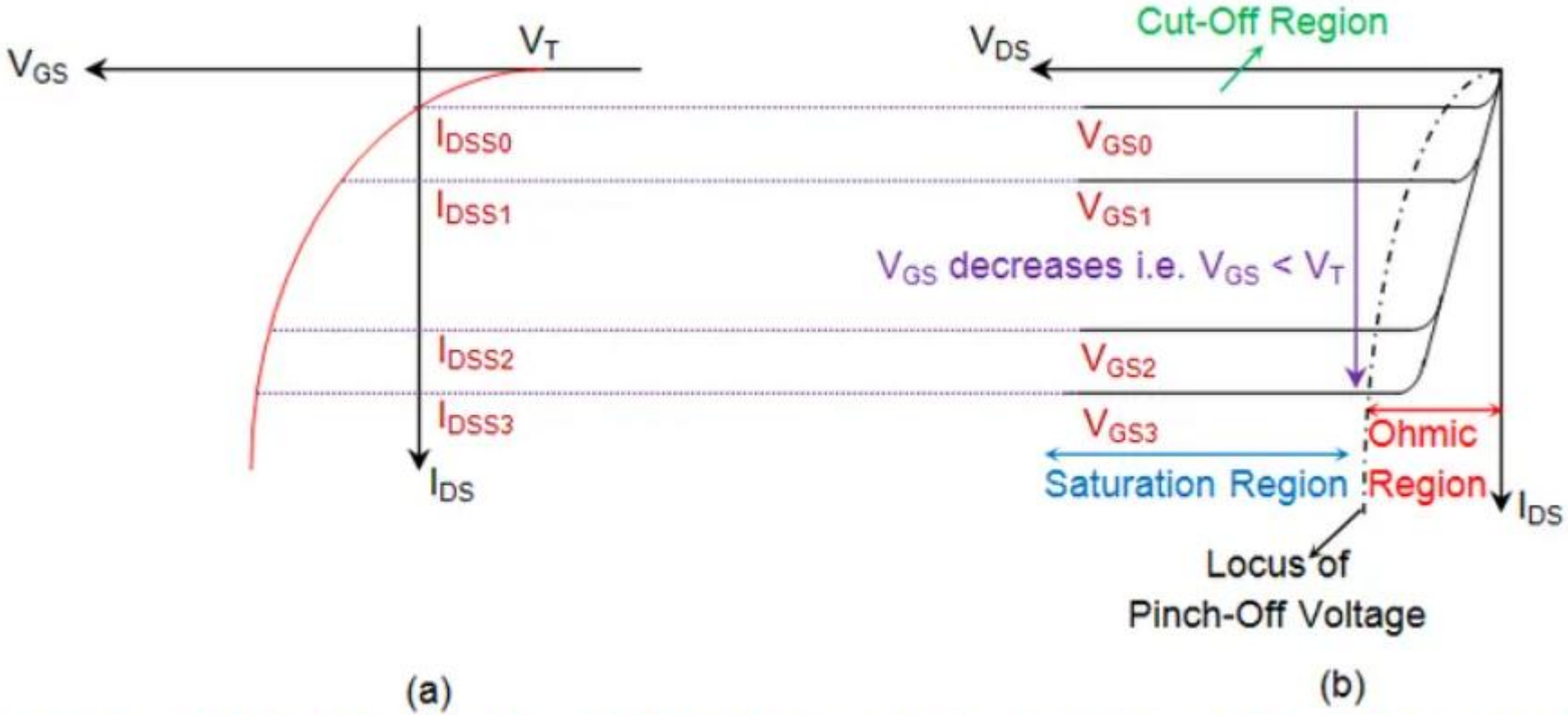


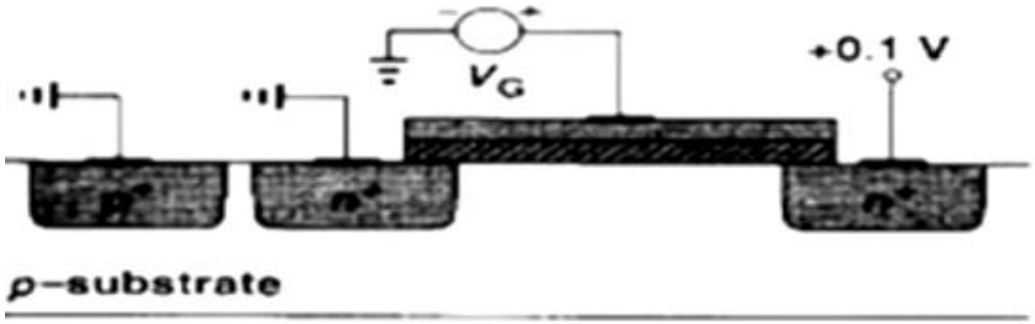
Figure 4 *p*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

The explanation provided above can be summarized in the form of a following table

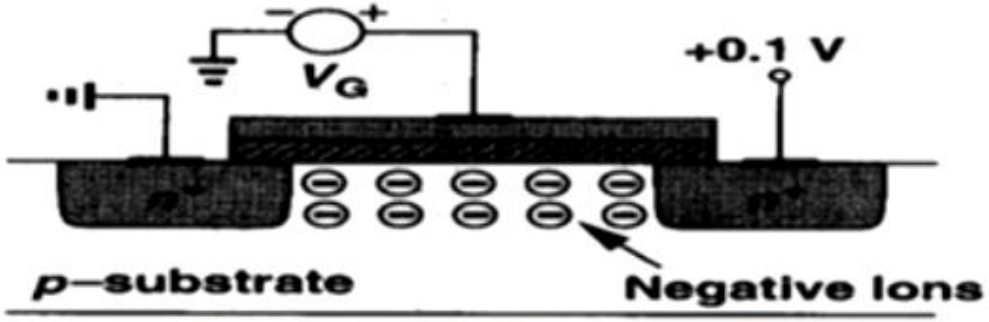
Kind of MOSFET	Region of Operation		
	Cut-Off	**Ohmic/Linear**	**Saturation**
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_P$	$V_{GS} > V_T$ and $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > -V_P$	$V_{GS} < -V_T$ and $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ and $V_{DS} < V_P$	$V_{GS} > -V_T$ and $V_{DS} > V_P$
p-channel Depletion-type	$V_{GS} > V_T$	$V_{GS} < V_T$ and $V_{DS} > -V_P$	$V_{GS} < V_T$ and $V_{DS} < -V_P$

Threshold Voltage of MOSFET

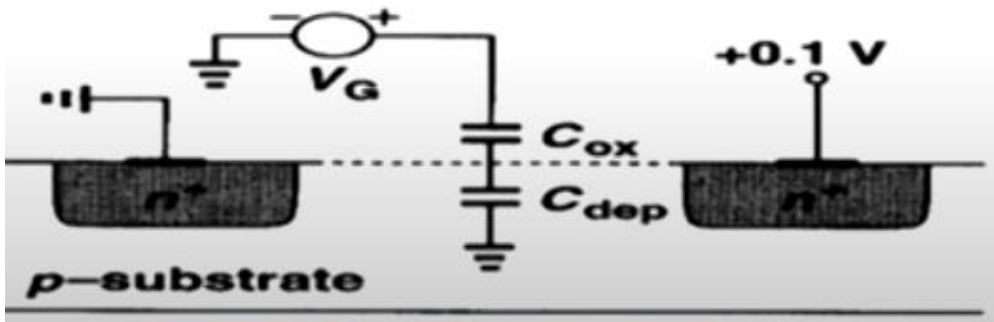
- With keeping constant drain bias, we'll analyze the different modes



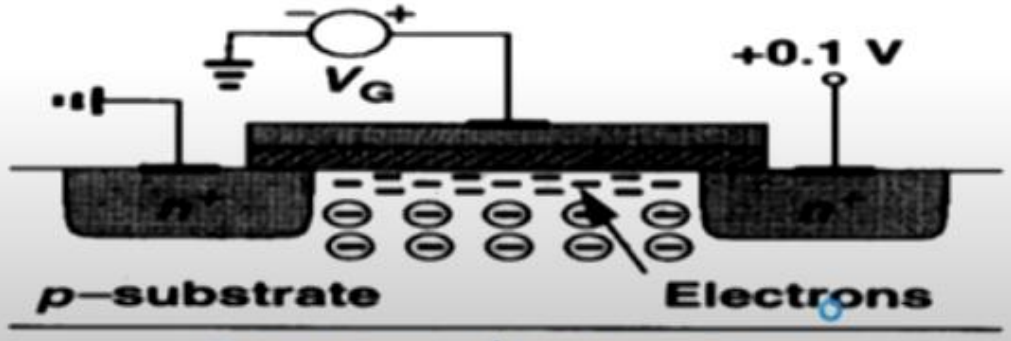
Device under consideration



Formation of Depletion Region



Onset of Inversion Layer



Formation of Inversion Layer

- As the gate and substrate forms a capacitor, the applied V_G images a opposite charge on the substrate.
- The increase in V_G increases the drop across gate-oxide and also the width of depletion region. Therefore, depletion capacitance (C_{dep}) and oxide capacitance (C_{ox}) are in series.
- Now, what would be the threshold value?

➢ The value of minimum gate voltage which inverts the surface, and hence an effective channels gets formed.

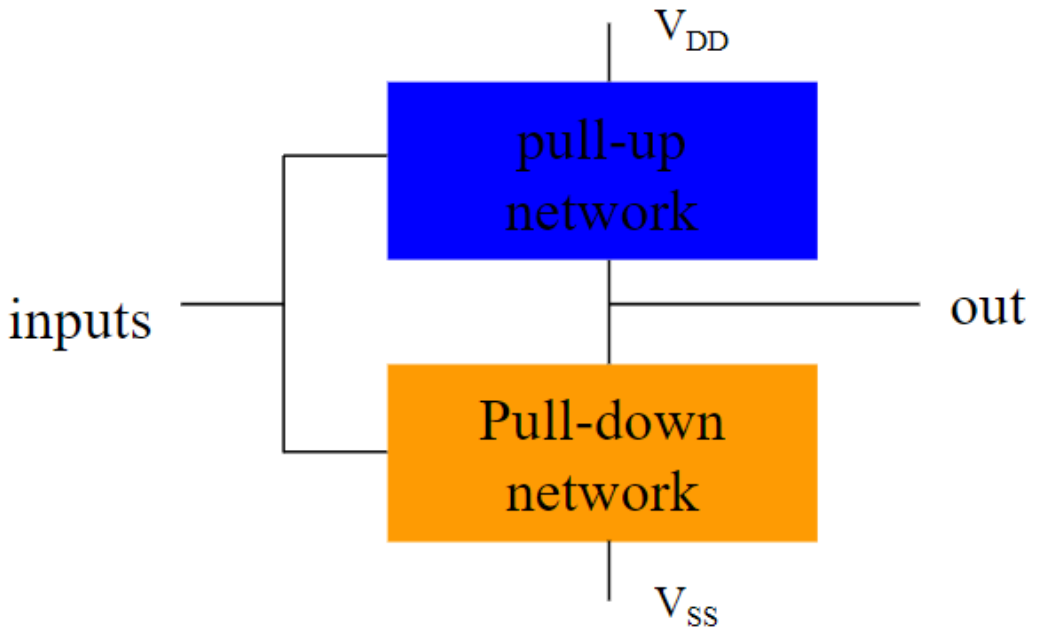
$$V_{TH}=\Phi_{MS}+2\Phi_F+\frac{Q_{dep}}{C_{ox}}$$

where $\Phi_{MS}=\Phi_M-\Phi_S$ is difference between metal and semiconductor work-functions

CMOS structure

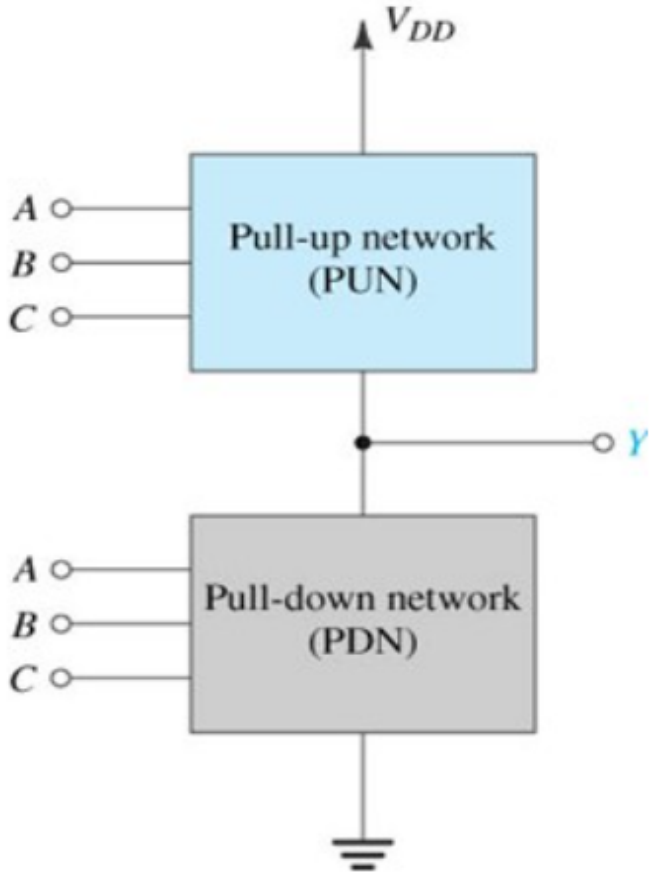
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS

Pull-up and pull-down networks



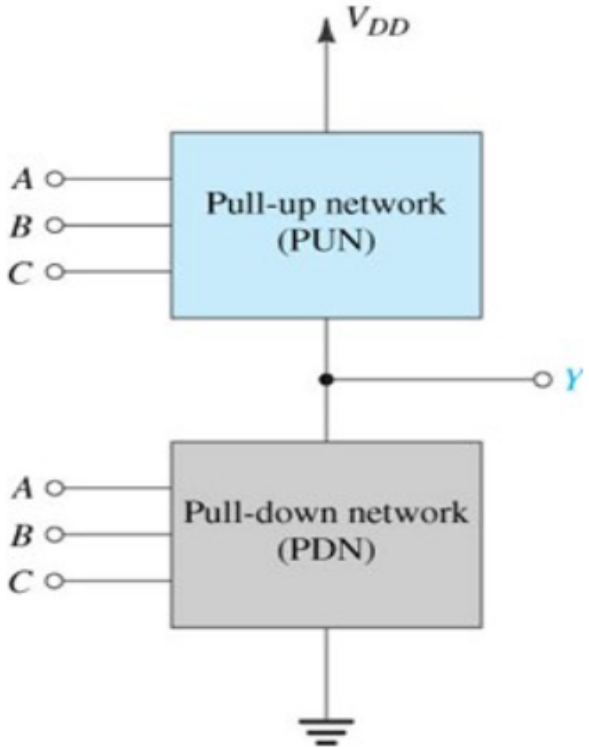
Basic structure

- When All Three input combinations are High **PDN** will conduct and will Pull the output node down to Ground making Output Low (Y=0) (Voltage Zero)
- Simultaneously, PUN will be OFF and no path will Exists between V_{DD} and Ground



Basic structure

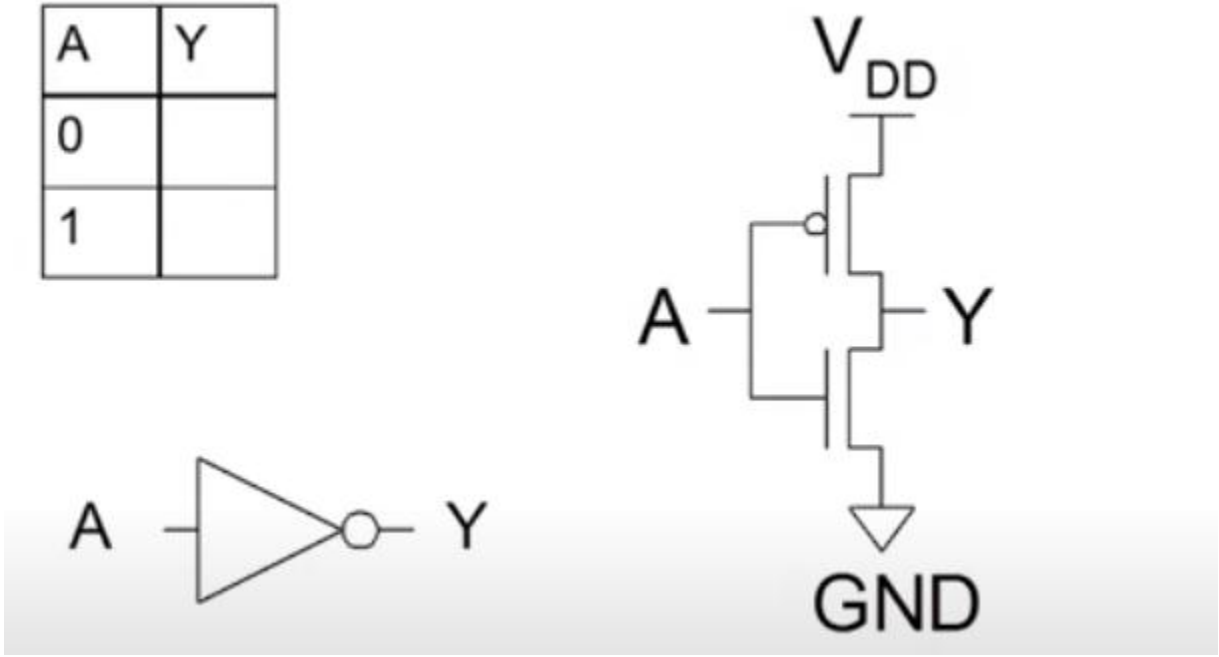
- When All Three input combinations are Low **PUN** will conduct and will Pull the output node Up to V_{DD} making Output High (Y=1) (Voltage = V_{DD})
- Simultaneously, PDN will be OFF and no path will Exists between V_{DD} and Ground



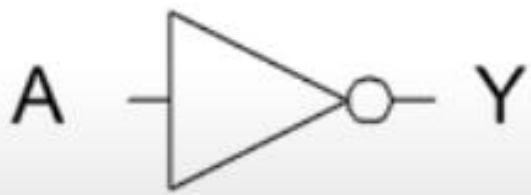
CMOS Inverter

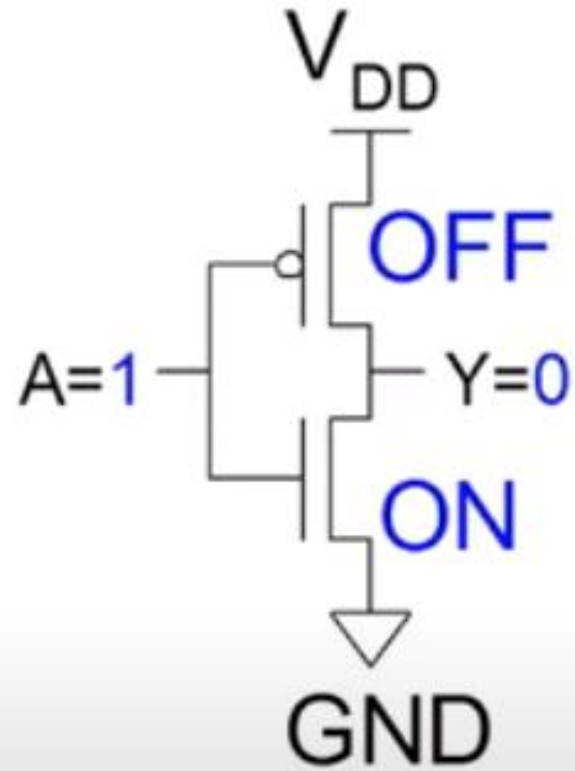
-

A	Y
0	
1	

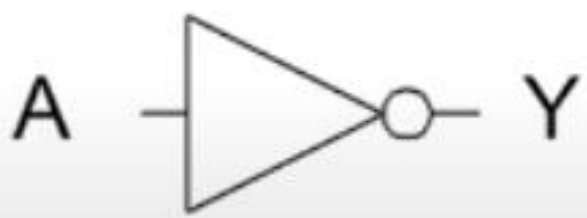


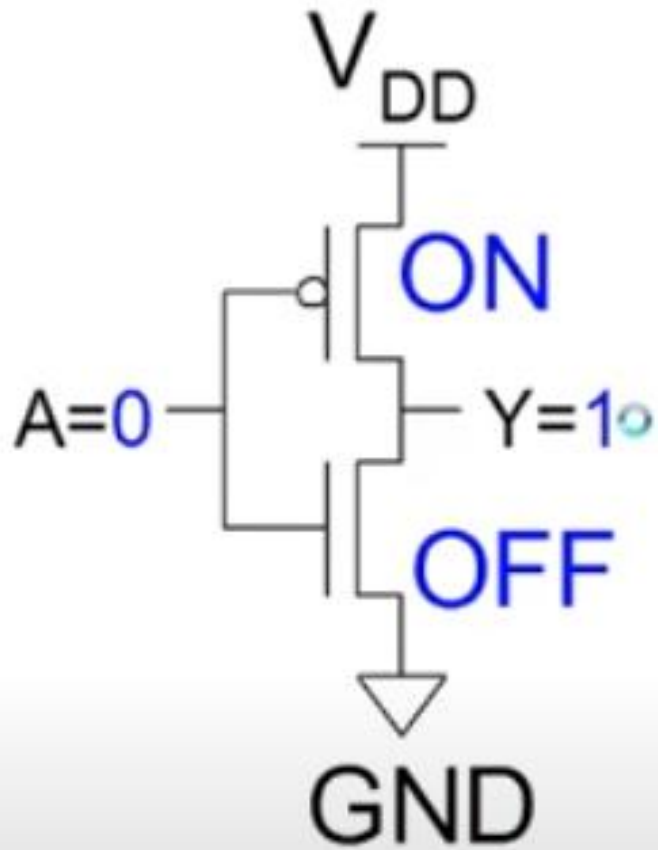
A	Y
0	
1	**0**



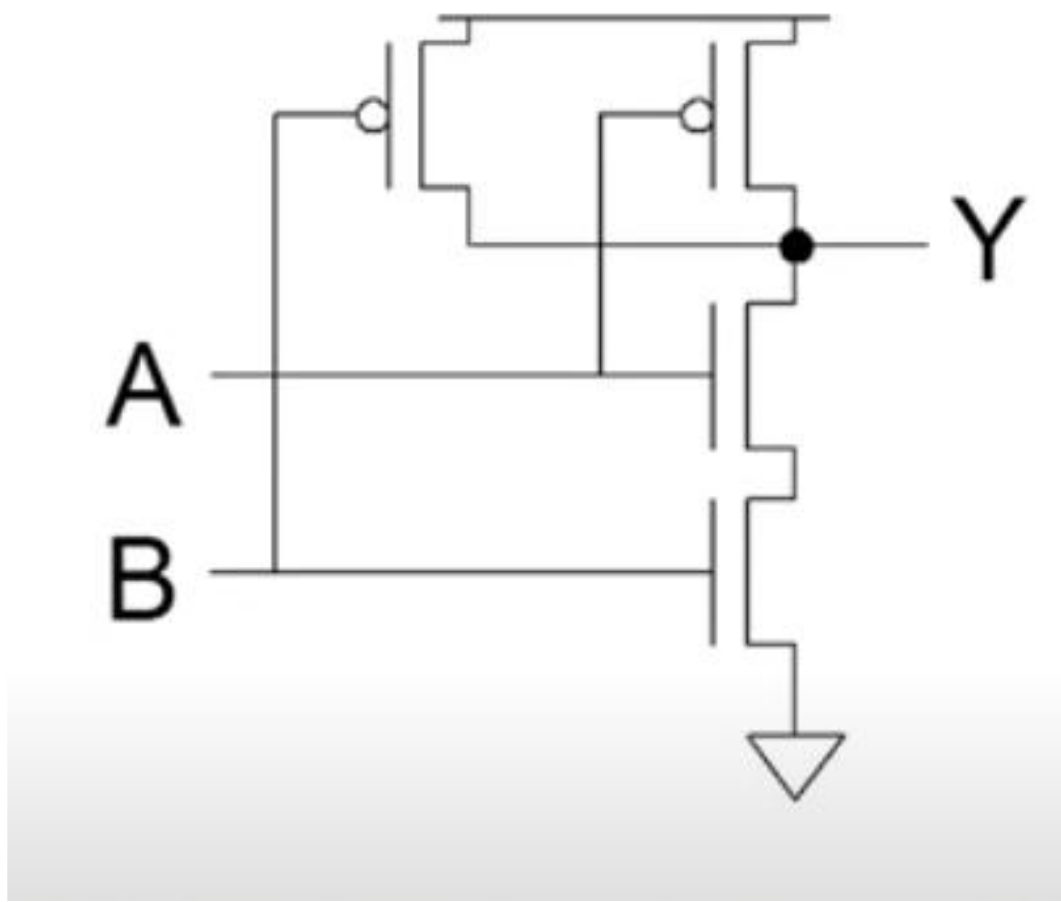


A	Y
0	1
1	0





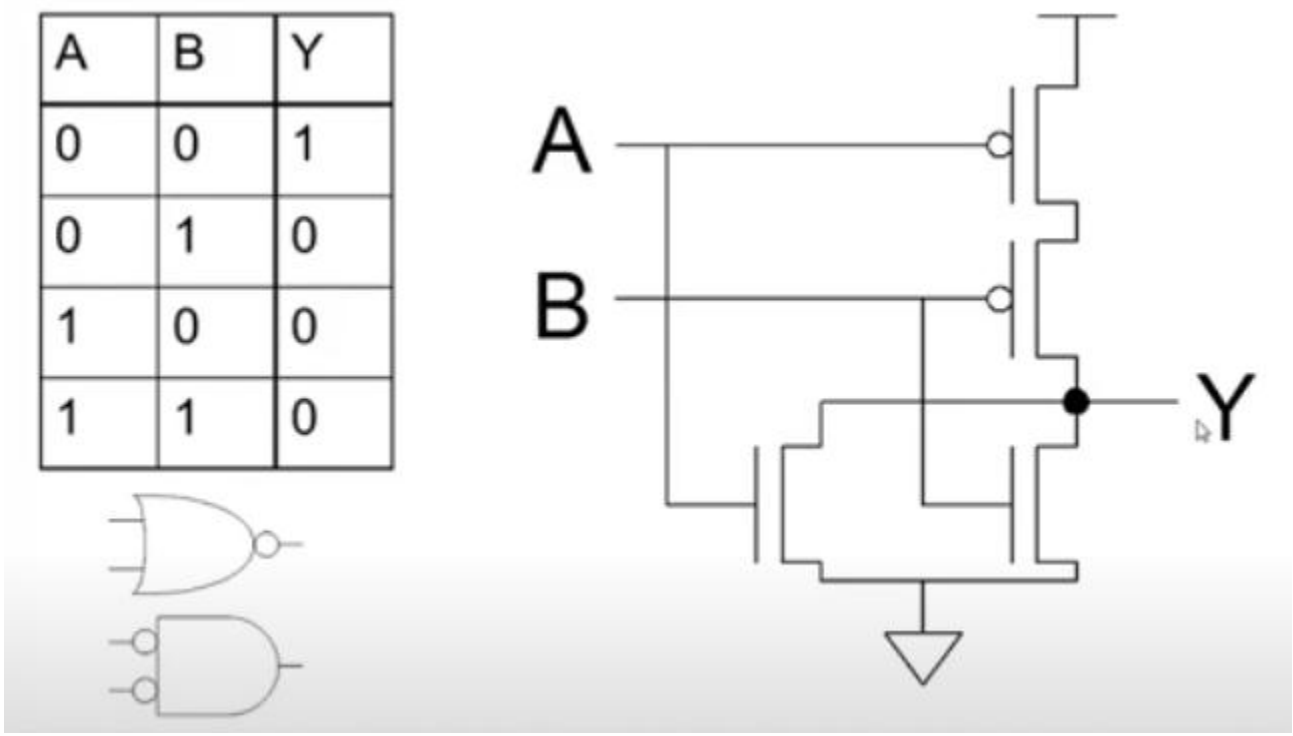
A	B	Y
0	0	
0	1	
1	0	
1	1	



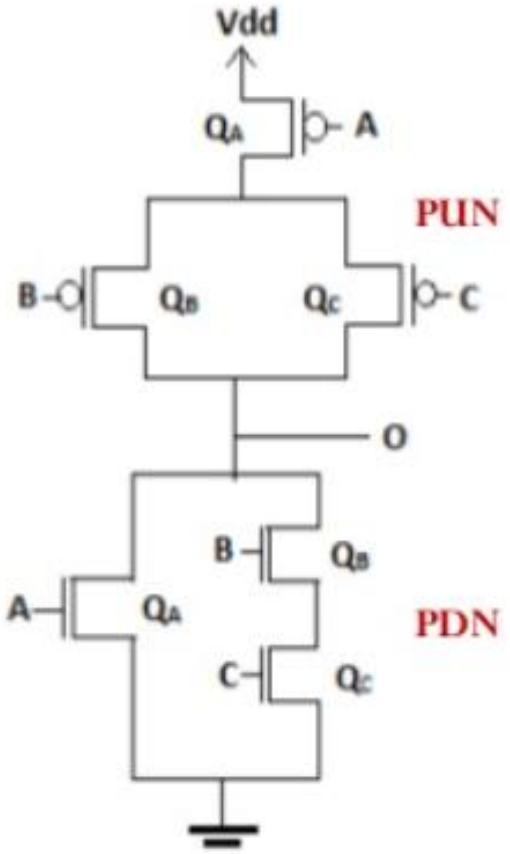
NOR gate

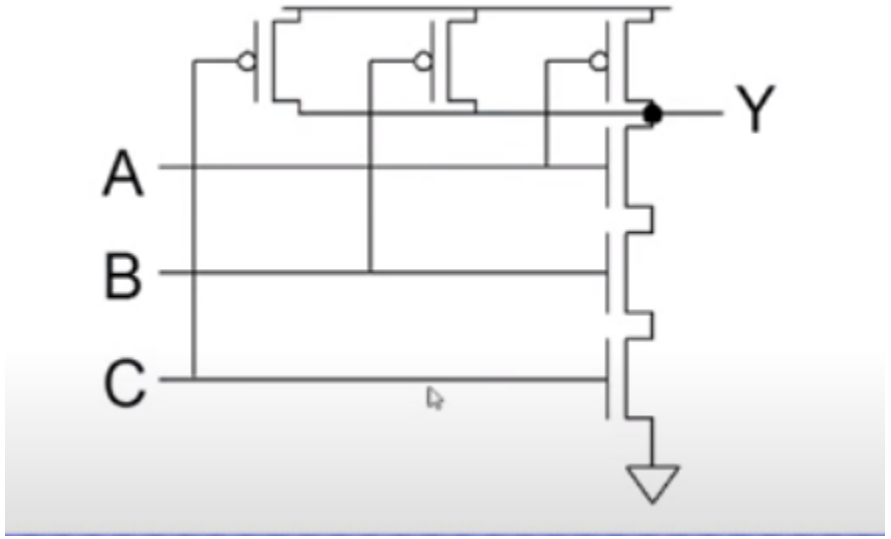
•

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Basic structure

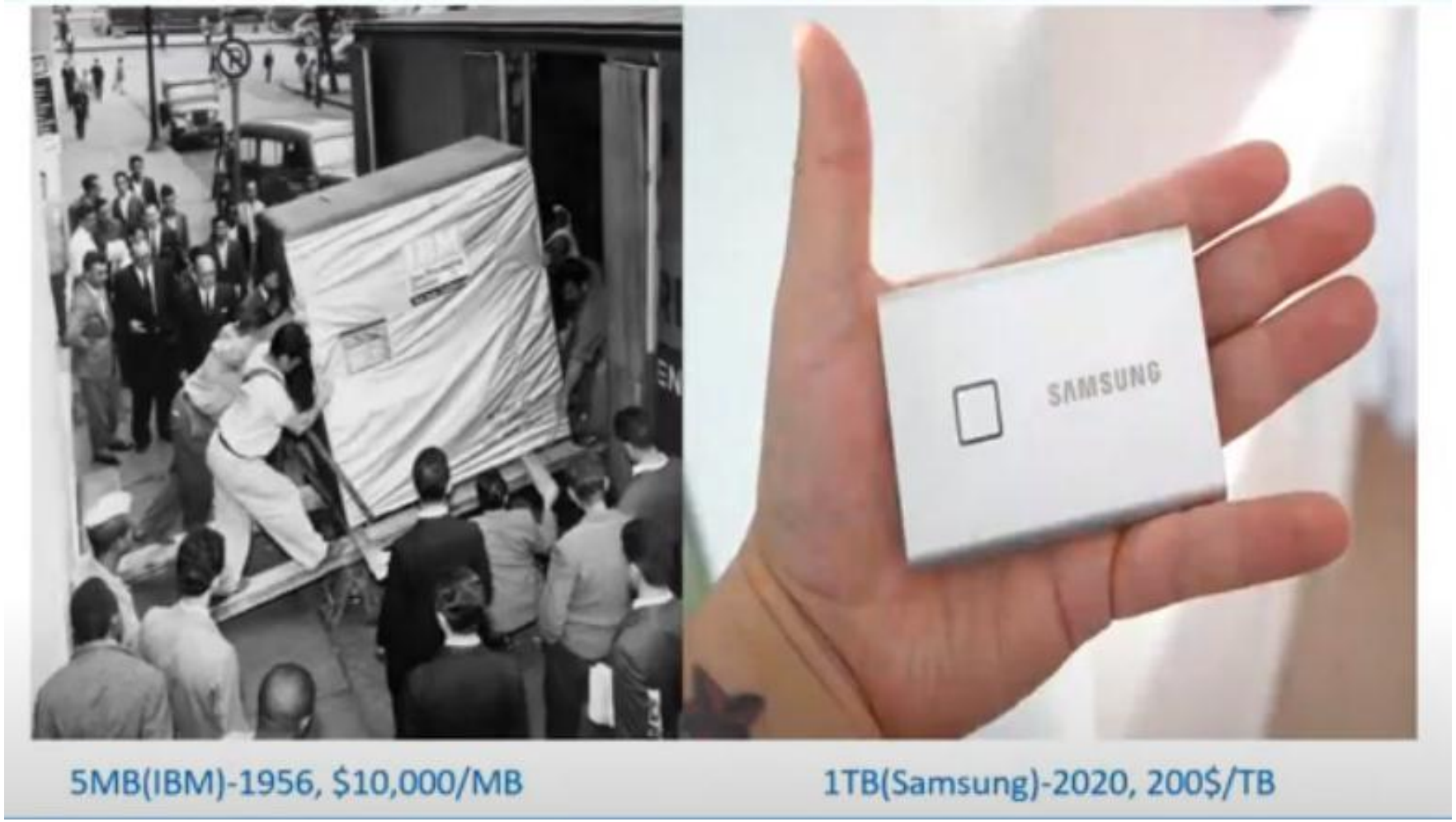




Guess this device?

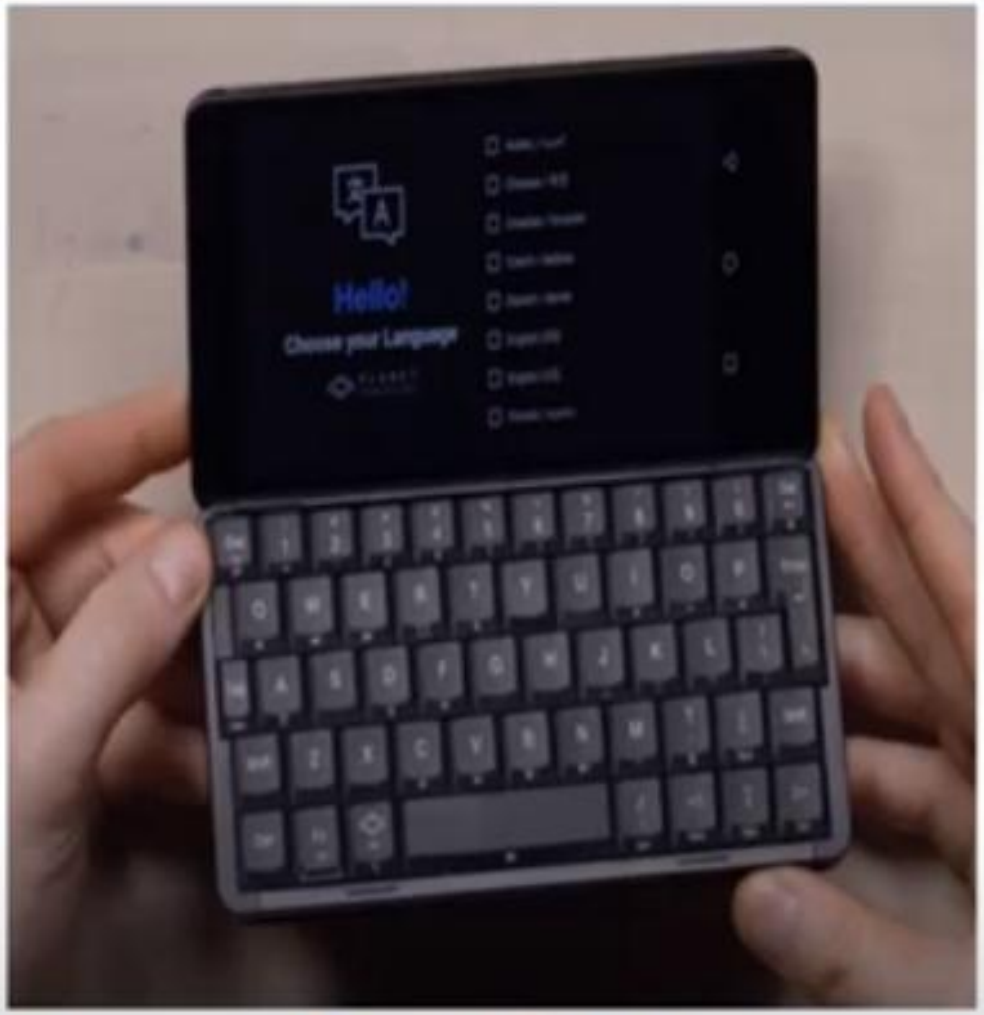
5 MB Hard disk by IBM IN 1956

Advancement due to VLSI



Achieved through VLSI

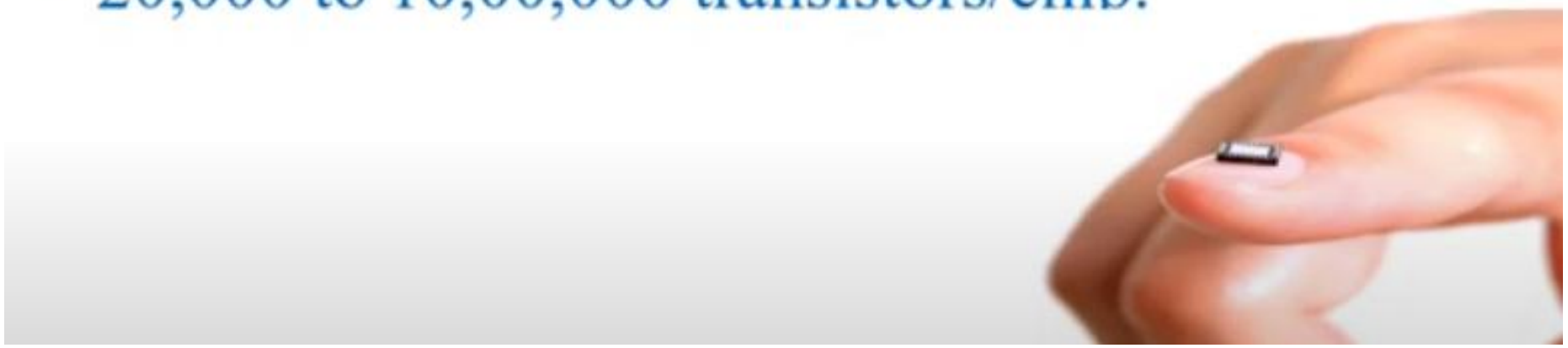
ENIAC-Worlds first electronic computer(1946)



Computer in 2020

Very Large Scale Integration

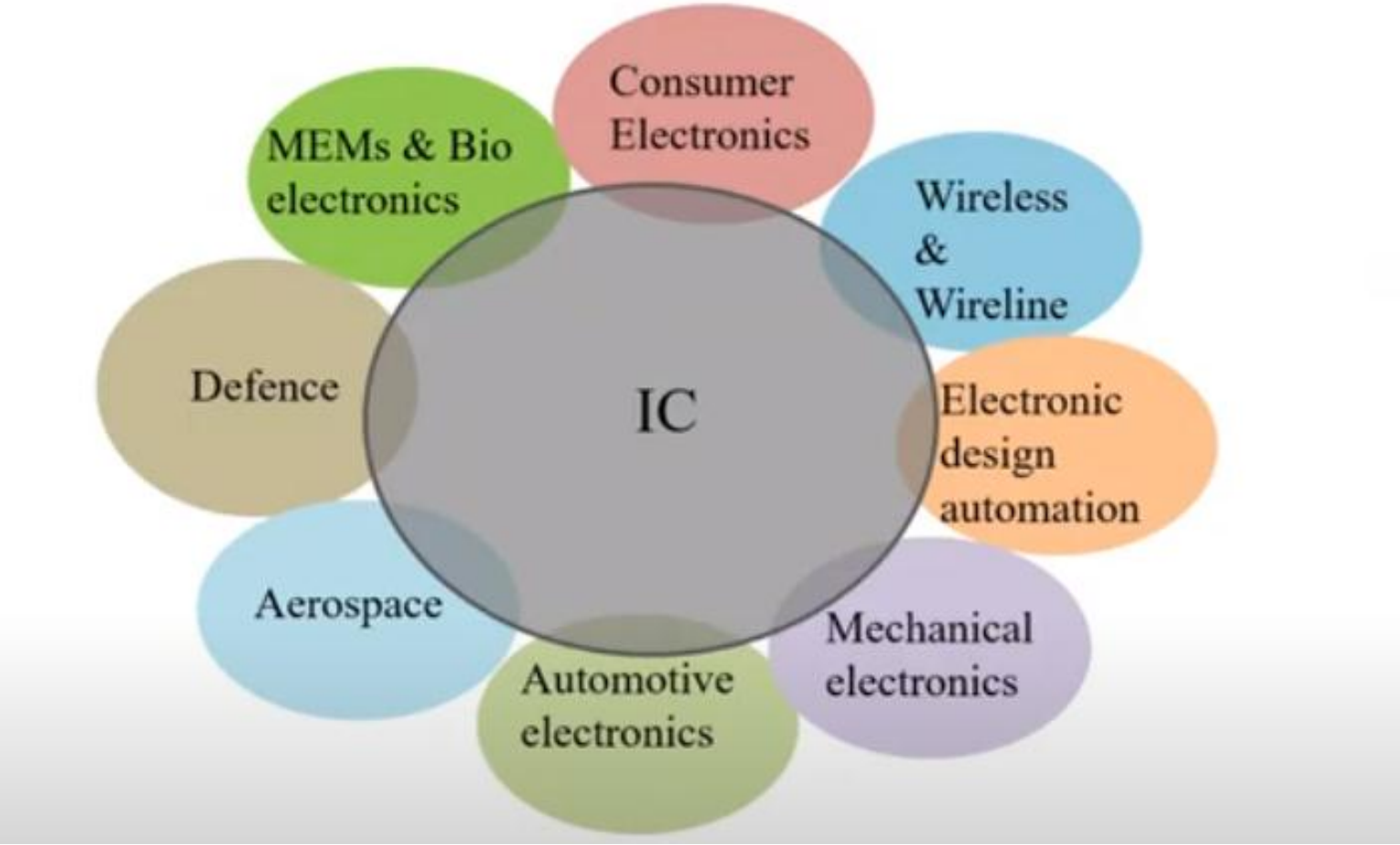
- VLSI is the process of creating Integrated Circuits by combining millions of transistors on single chip.
- Invented in 1980.
- 20,000 to 10,00,000 transistors/chip.



Why VLSI?

- Physical size of device can be reduced
- Effective cost of the devices can be reduced
- The operating speed of circuit is increased
- Requires less power
- Higher reliability
- Easier to design

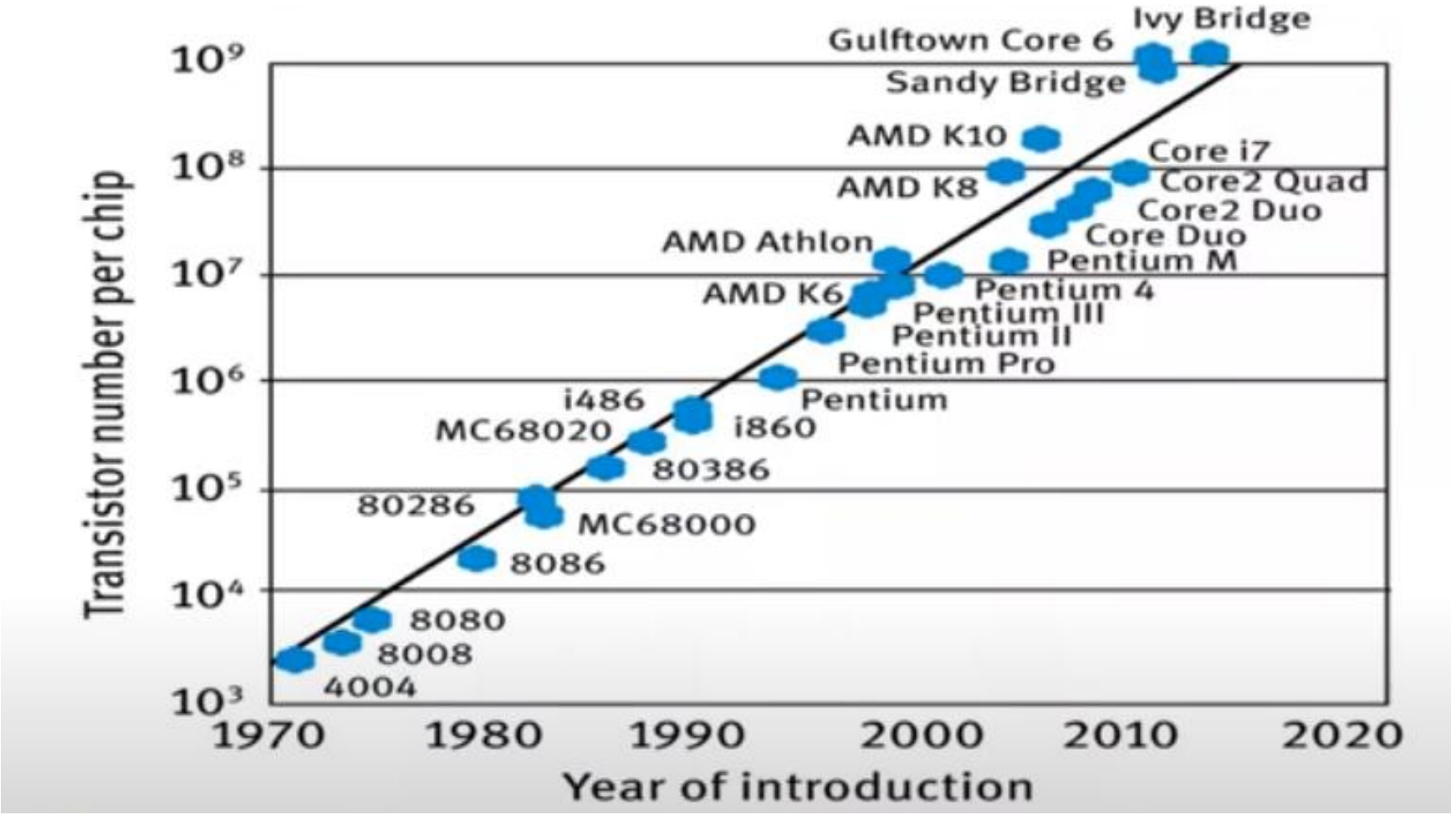
Application of ICs



IC Evolution

- SSI-Small Scale Integration-1960
  - Less than10 logic gates/chip
  - Logic gates(AND,OR,NAND,NOR)
- MSI-Medium Scale Integration-1966
  - 10 to 100 gates/chip
  - Flip flops, adders, counters, multiplexers
- LSI-Large Scale Integration-1970
  - 100 to 10,000 gates/chip
  - Small memory chips, Programmable Logic Devices
- VLSI- Very Large Scale Integration(1980)
  - 10,000 to 100,000 gates/chip
  - Micro processors, now offer 64-bit processor complete with cache memory, floating point arithmetic units, RAM,ROM, complex PLDs.

Moore's Law


Transistor number per chip
10^9
10^8
10^7
10^6
10^5
10^4
10^3
1970
1980
1990
2000
2010
2020
Year of introduction
Ivy Bridge
Gulftown Core 6
Sandy Bridge
AMD K10
Core i7
AMD K8
Core2 Quad
Core2 Duo
Core Duo
AMD Athlon
Pentium M
AMD K6
Pentium 4
Pentium III
Pentium II
Pentium Pro
Pentium
i486
i860
MC68020
80386
80286
MC68000
8086
8080
8008
4004

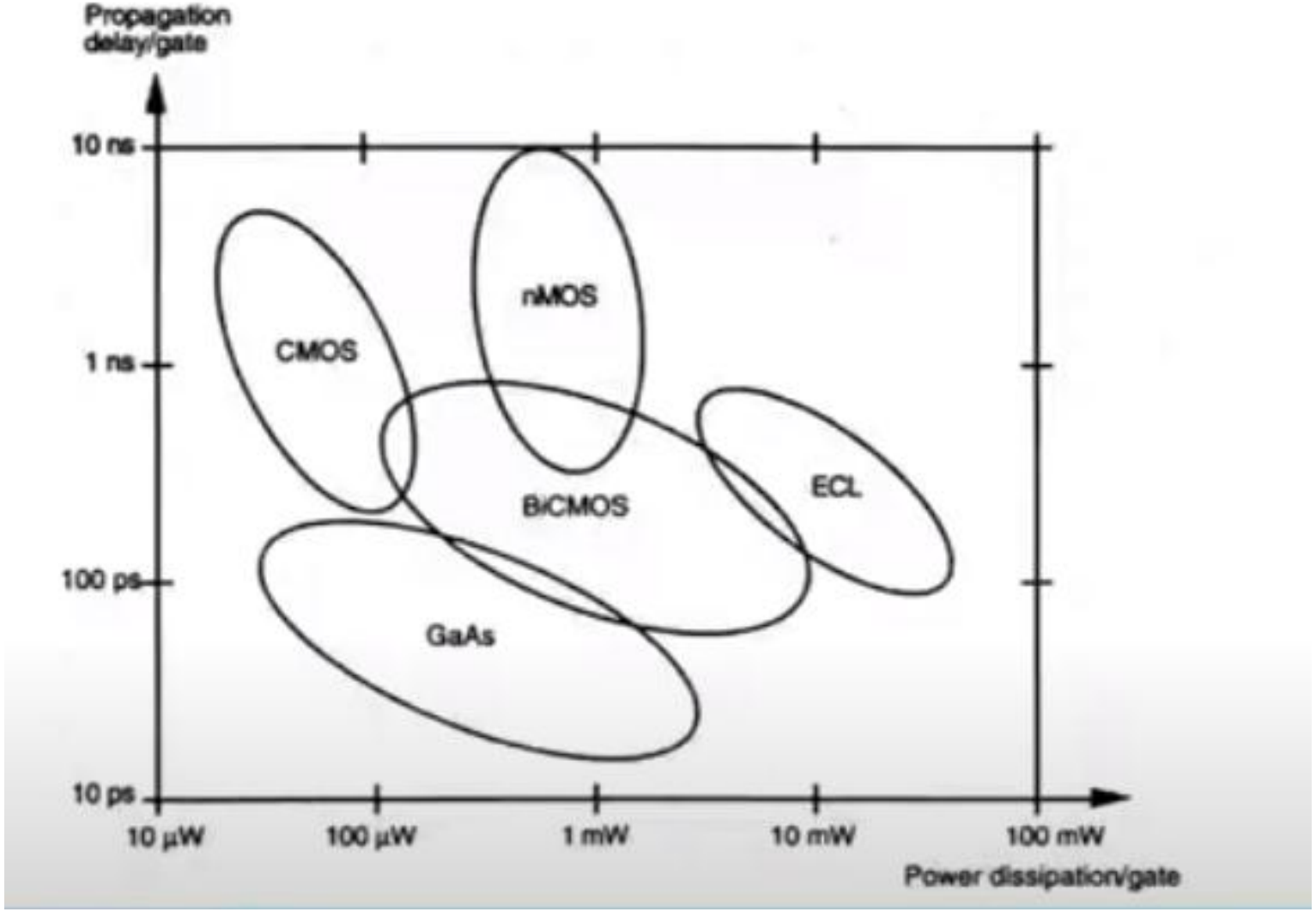
Moore’s Law (cont..)

- The number of transistors on an integrated circuit will double every 18 months
- In 1965, Gordon Moore, co founder of Intel, predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months
  - i.e., grow exponentially with time
  - 2300 transistors, 1 MHz clock (Intel 4004) – 1971
  - 2.16 Billion transistors,126sq.mm, 2.9GHz (Intel i7) -2009

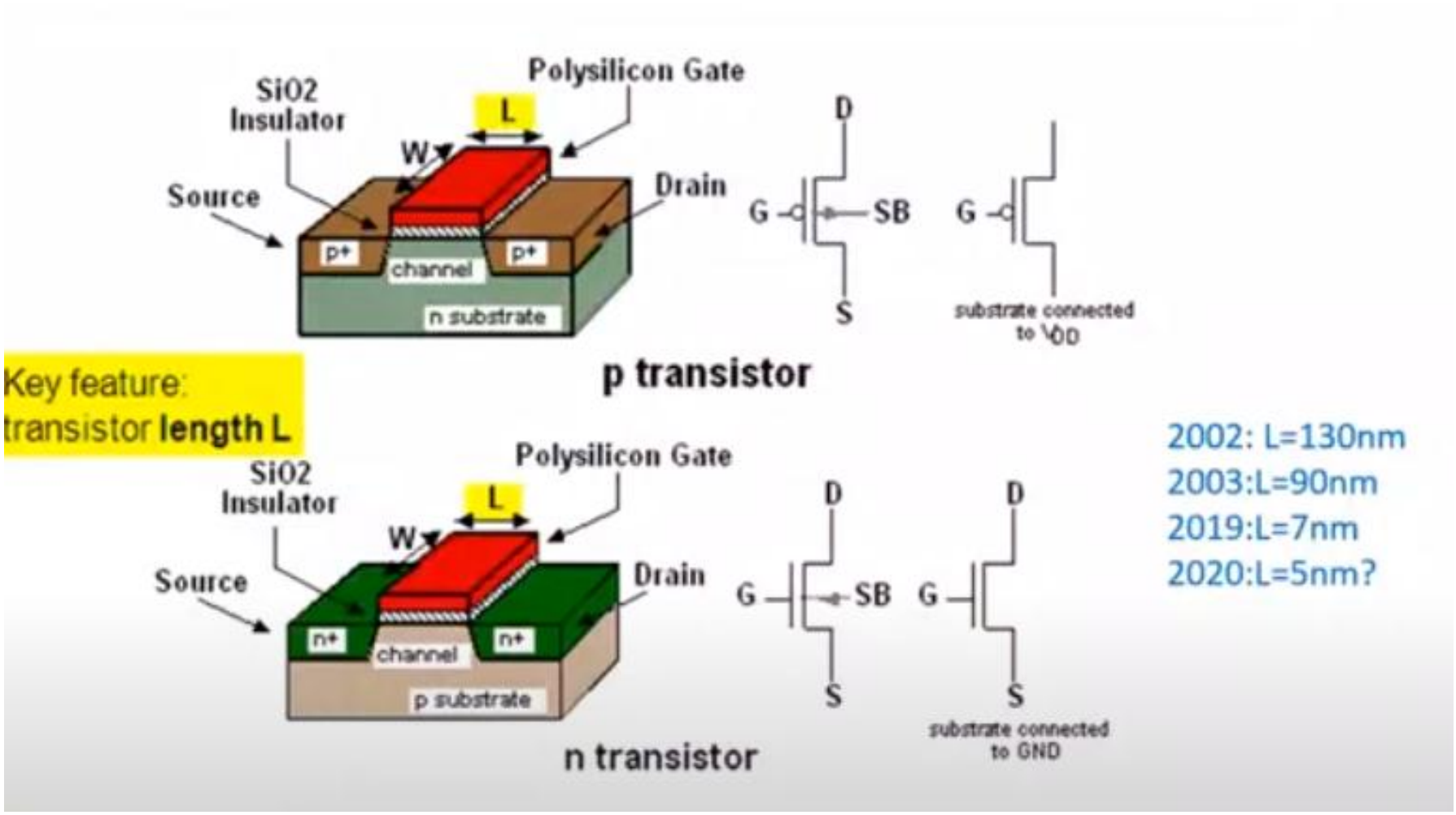
Processing technologies of VLSI

- Bipolar
  - TTL(Transistor to Transistor Logic)
  - ECL(Emitter Coupled Logic)
- MOS(Metal Oxide Semiconductor)
  - NMOS(N-channel)-Less masking steps, denser, less power
  - CMOS(Complementary): N-Channel & P-channel MOS transistors, Low power consumption, less fabrication steps
- BiCMOS: Bipolar and CMOS(for high speed)
- Ga-As: Gallium Arsenide (for high speed)
- SOI: Silicon On Insulator(for high temperature applications)

Power dissipation & propagation delay



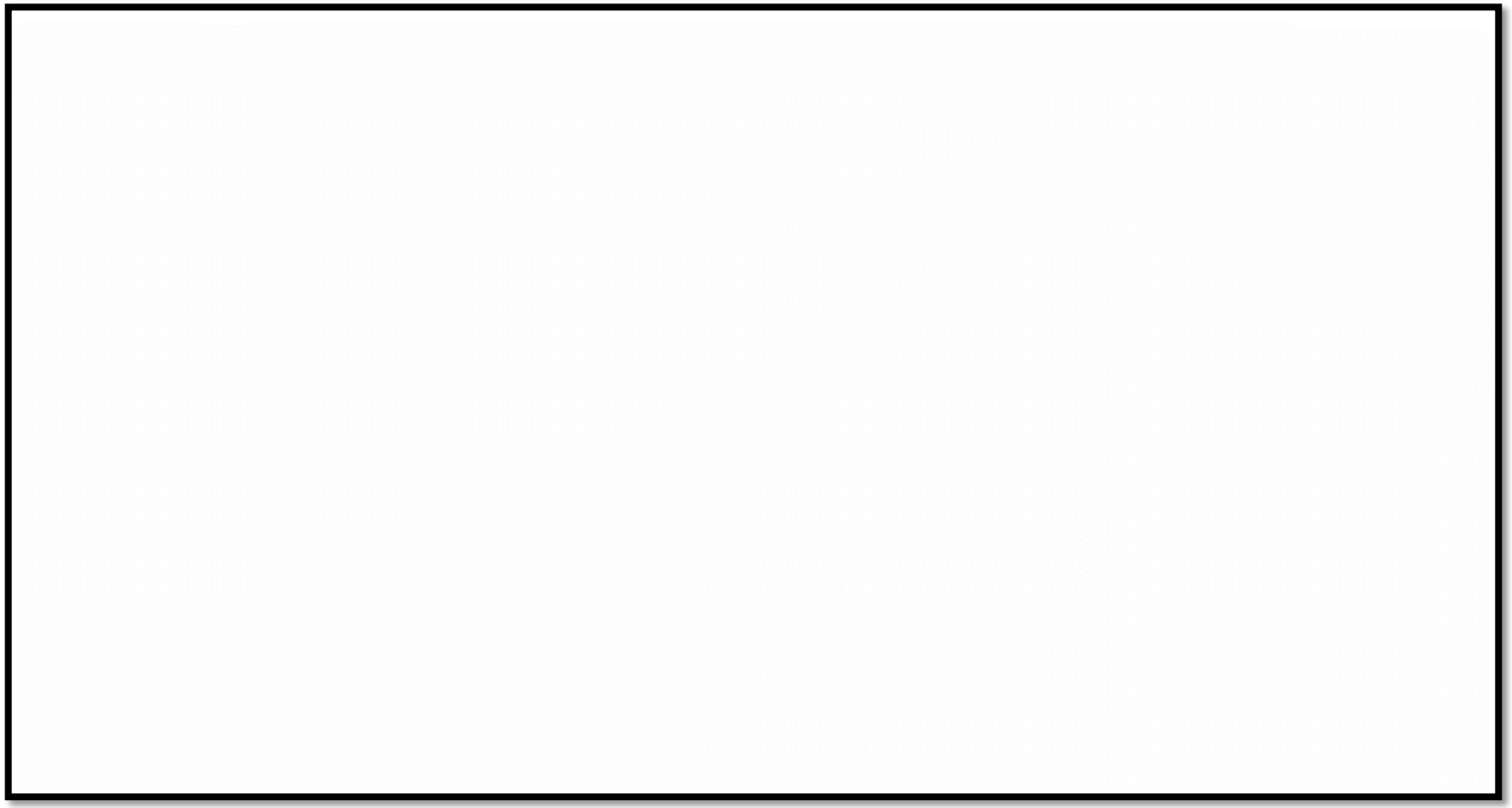
N MOS &PMOS transistors



IC fabrication process

- Silicon Wafer manufacturing
- Wafer processing
  - Oxidation
  - Photo Lithography
  - Etching
  - Diffusion & Ion implantation
  - Metallization
- Testing
- Assembly and packaging

IC Fabrication process-Video from Intel

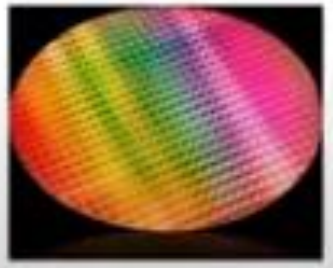


Creating wafers

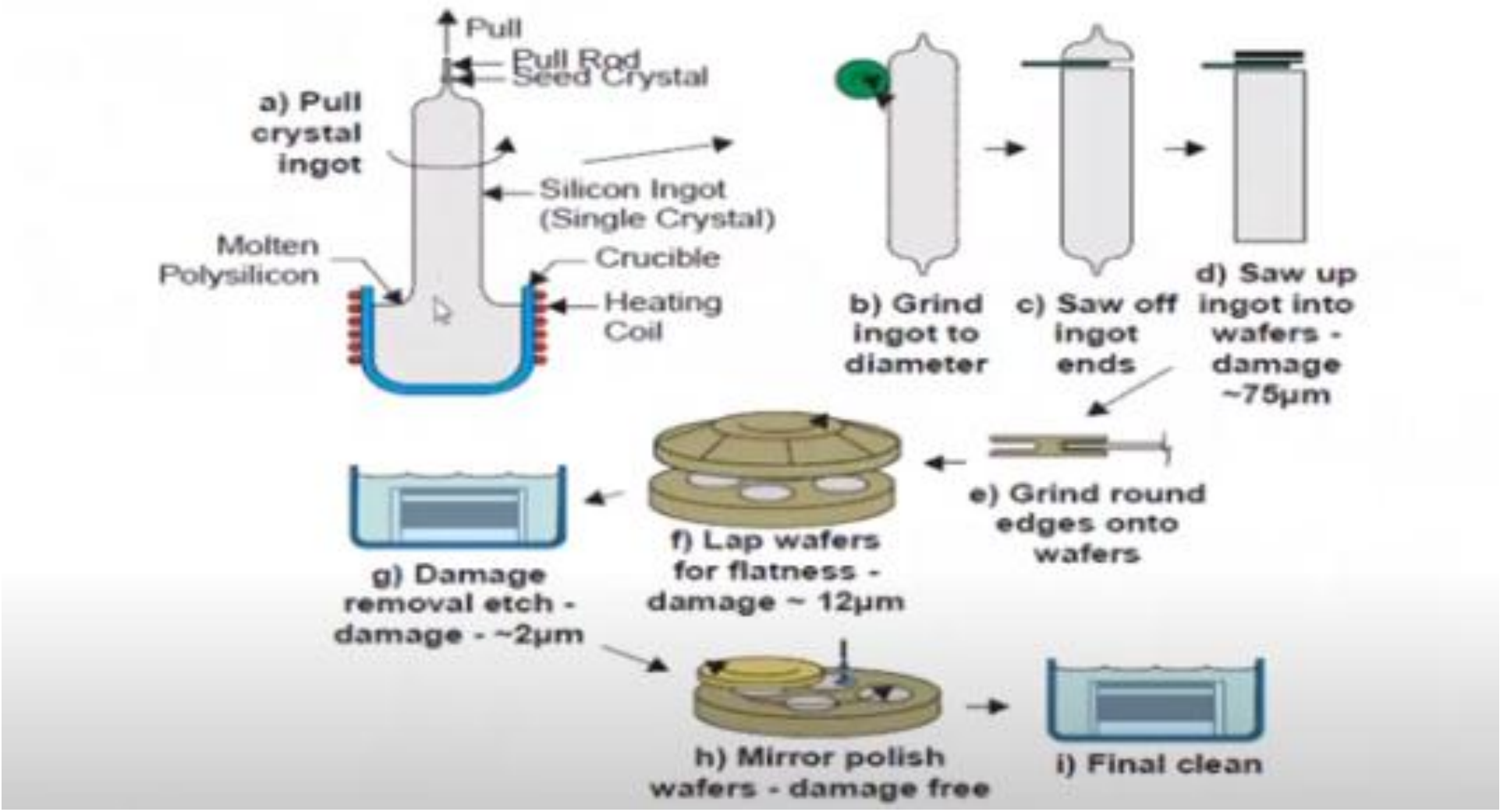
Silicon in nature

•Czochralski Method

Single Crystal Silicon Ingot



Silicon wafer manufacturing process



Oxidation

- The process by which a layer of silicon di oxide is grown

1. Wet Oxidation $Si + 2H_2O \xrightarrow{900^\circ C} SiO_2 + 2H_2 \uparrow$
   - Water vapour
   - Used to grow Thick Oxide

2. Dry Oxidation $Si + O_2 \xrightarrow{1200^\circ C} SiO_2$
   - Oxygen gas
   - Used to grow Thin Oxide

- Thickness depends on Temperature and Time

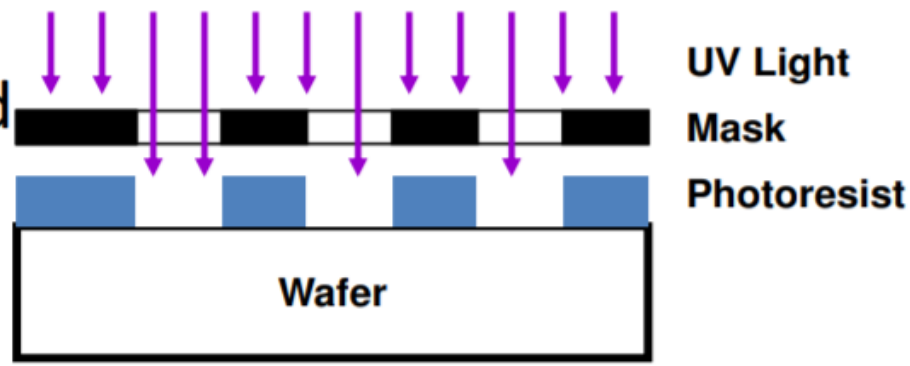
- Formation of silicon dioxide layer on the surface of Si wafer
  1. protects surface from contaminants
  2. forms insulating layer between conductors
  3. form barrier to dopants during diffusion or ion implantation
  4. grows above and into silicon surface

- Dry oxidation: lower rate and higher quality
- Wet oxidation: higher rate and lower quality

1. SiO_2 is an extremely hard protective coating & is unaffected by almost all reagents except by hydrochloric acid. Thus it stands against any contamination.
2. By selective etching of SiO_2, diffusion of impurities through carefully defined through windows in the SiO_2 can be accomplished to fabricate various components.

Photolithography

- Coat wafer with photoresist (PR)
- Shine UV light through mask to selectively expose PR
- Use acid to dissolve exposed PR
- Now use exposed areas for
  - Selective doping
  - Selective removal of material under exposed PR



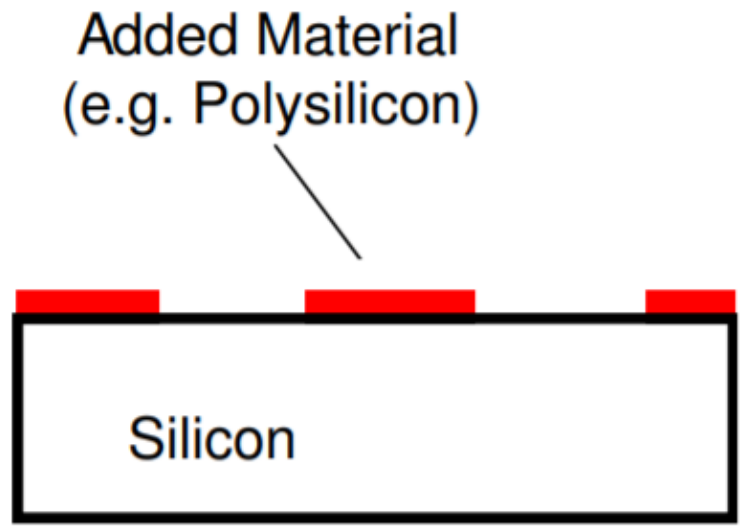
NMOS FABRICATION PROCESS

1.Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown. Such wafers are typically 75 to 150 mm in diameter and 0.4 mm thick and are doped with, say, boron to impurity concentrations of 1015/cm3 to 1016/cm3 , giving resistivity in the approximate range 25 ohm cm to 2 ohm cm.

STEP-1

Patterning Materials using Photolithography

- Add material to wafer
- Coat with photoresist
- Selectively remove photoresist
- Remove exposed material
- Remove remaining PR



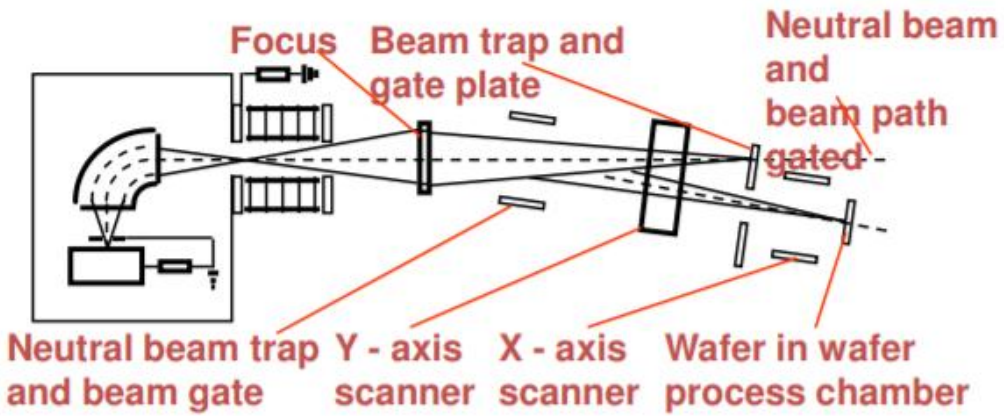
Ion Implantation

Process Conditions

Flow Rate: 5 sccm

Pressure: 10^{-5} Torr

Accelerating Voltage: 5 to 200 keV



Gases

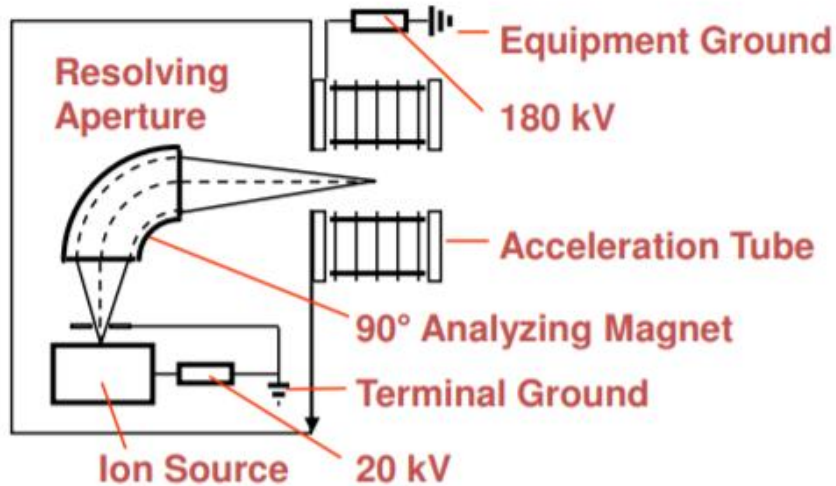
- Ar
- AsH_3
- $B^{11}F_3$ *
- He
- N_2
- PH_3
- SiH_4

Solids

- Ga
- In
- Sb

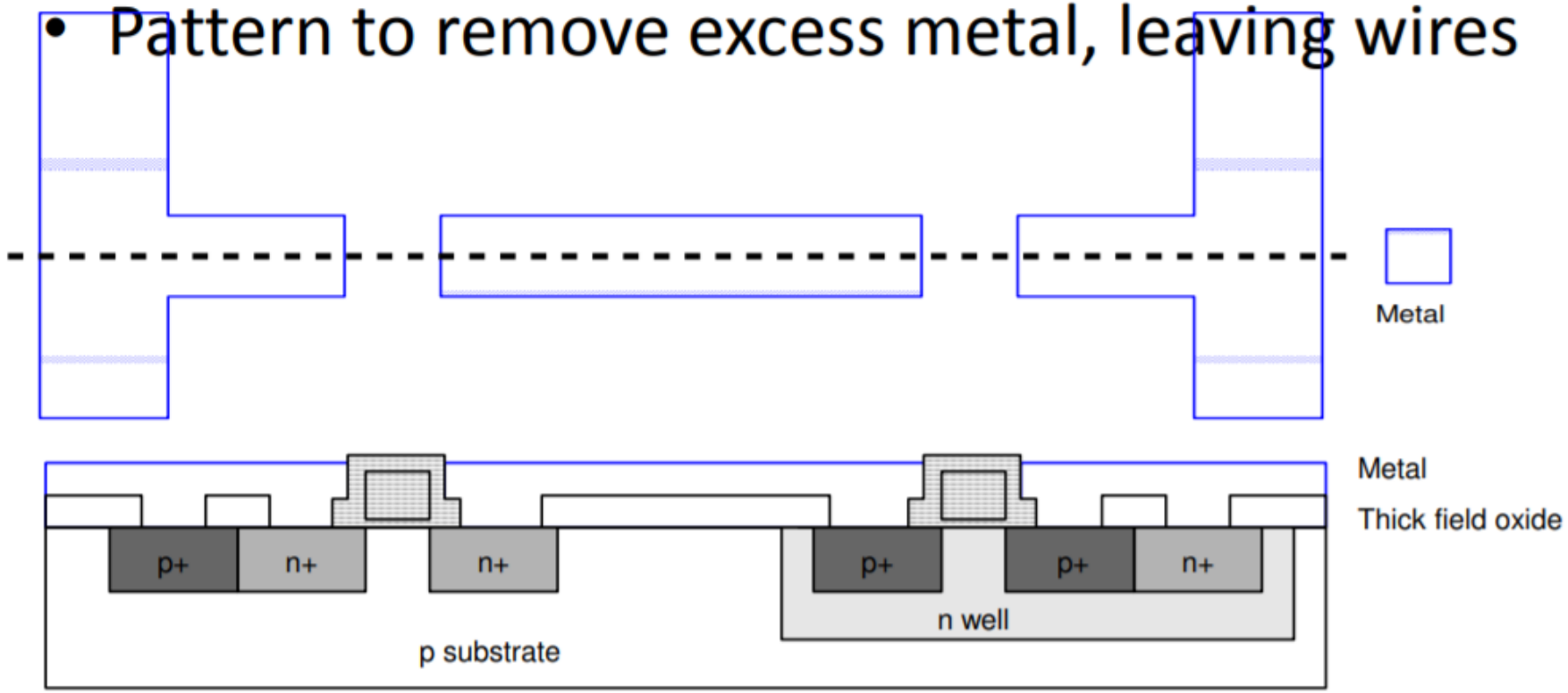
Liquids

- $Al(CH_3)_3$



Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



nMOS fabrication steps

1. Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown.

2. A layer of silicon dioxide (Si02) is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.

3. The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.

4. The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels.

5. These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.

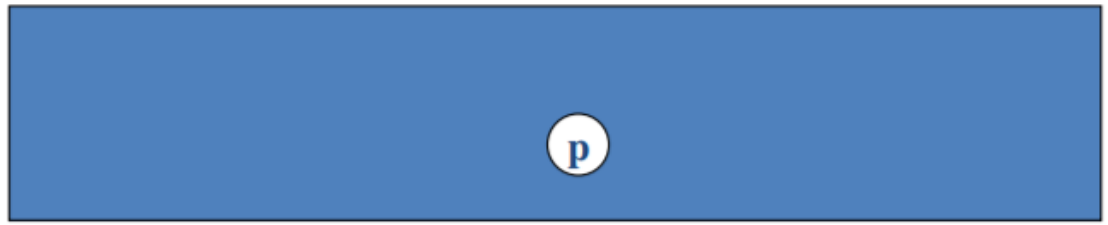
6. The remaining photoresist is removed and a thin layer of Si02 is grown over the entire chip surface and then polysilicon is deposited on top of this to form the gate structure.

7. Further photoresist coating and masking allows the polysilicon to be patterned (as shown in Step 6) and then the thin oxide is removed to expose areas into which

8. Thick oxide (Si02) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source areas where connections (i.e. contact cuts) are to be made.

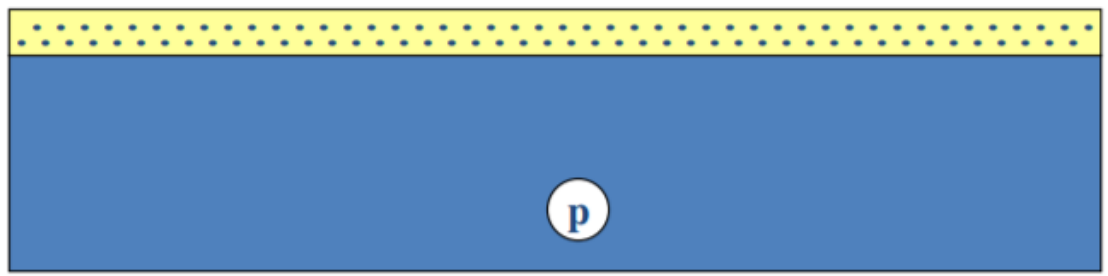
9. The whole chip then has metal (aluminium) deposited over its surface. This metal layer is then masked and etched to form the required interconnection pattern.

1.



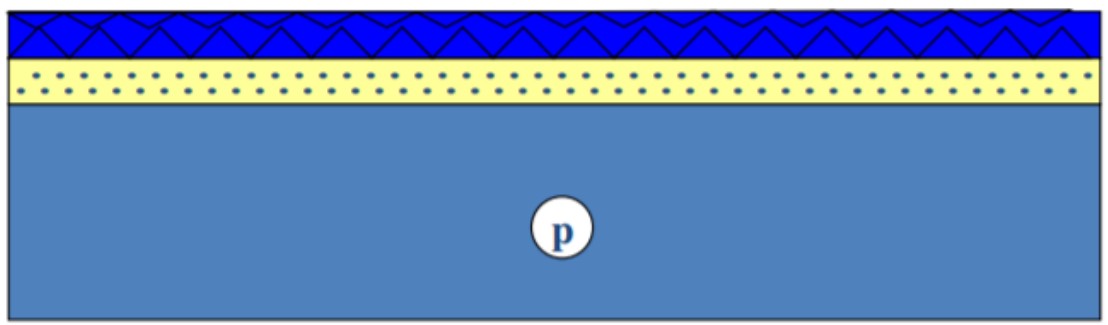
Substrate

2.

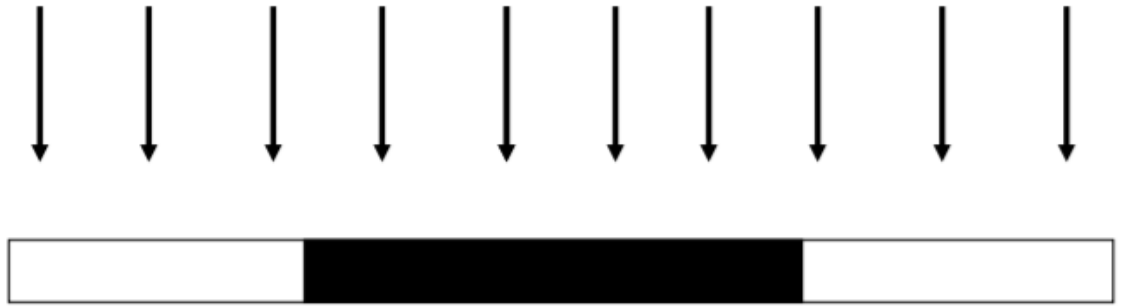


Thick oxide
(1μm)

3.



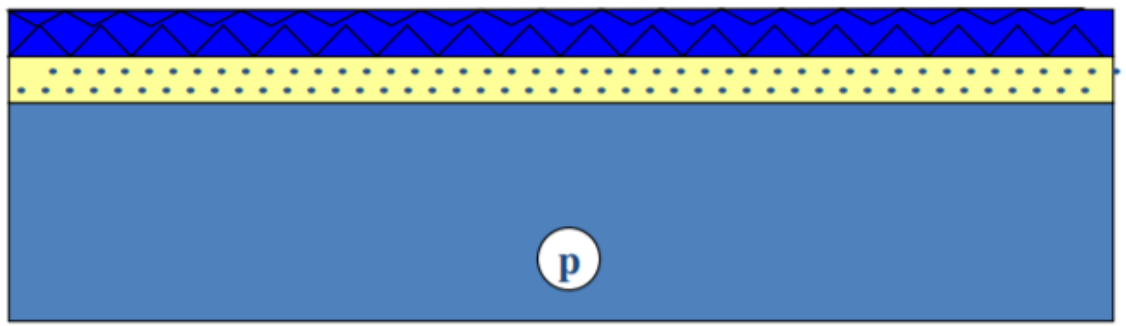
Photoresist



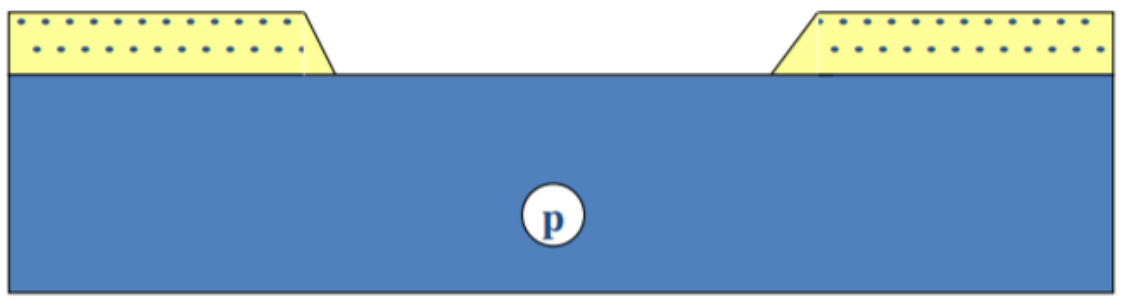
UV light

Mask

4.

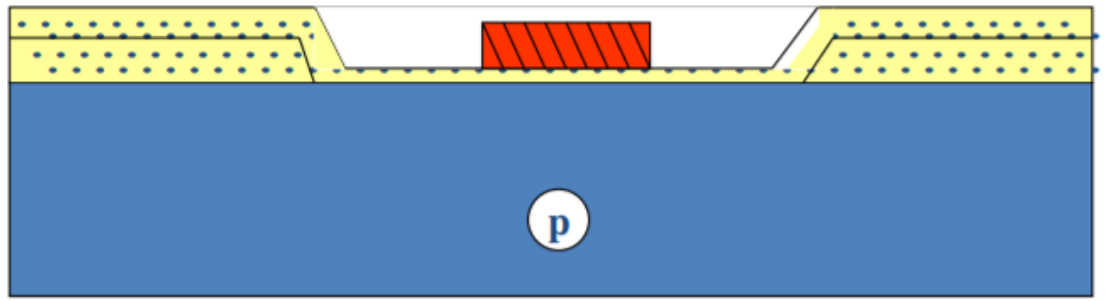


5.



Window in oxide

6.

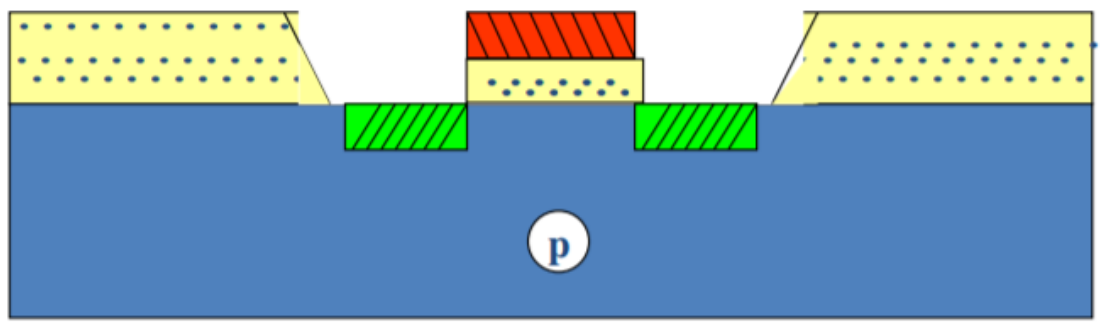


Patterned
Poly. (1-2 μm)

On thin oxide

(800-1000A^0)

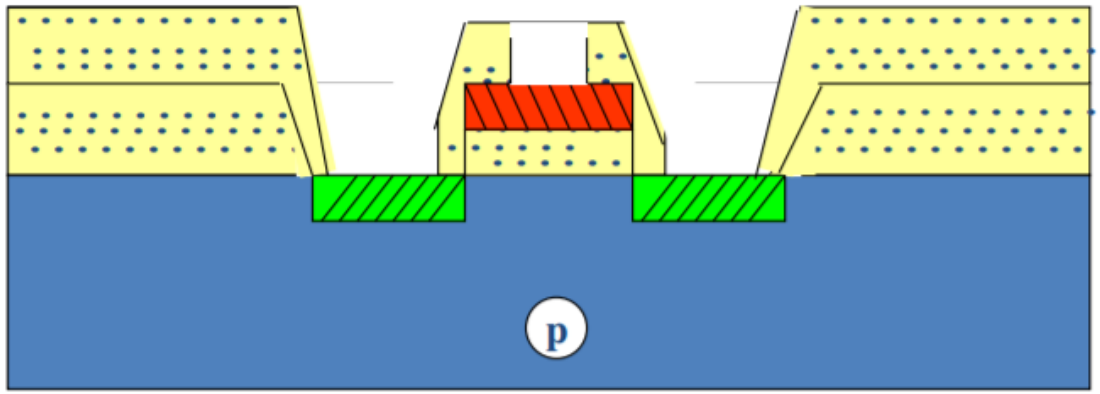
7.



n^+ diffusion

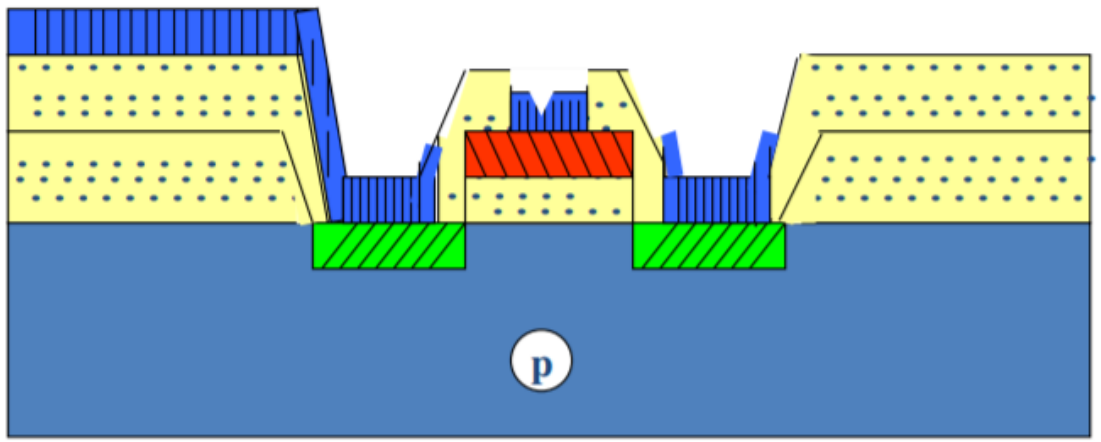
(1 μm deep)

8.



Contact holes (cuts)

9.



Patterned Metallization (aluminum 1 μm)

The p-well CMOS fabrication

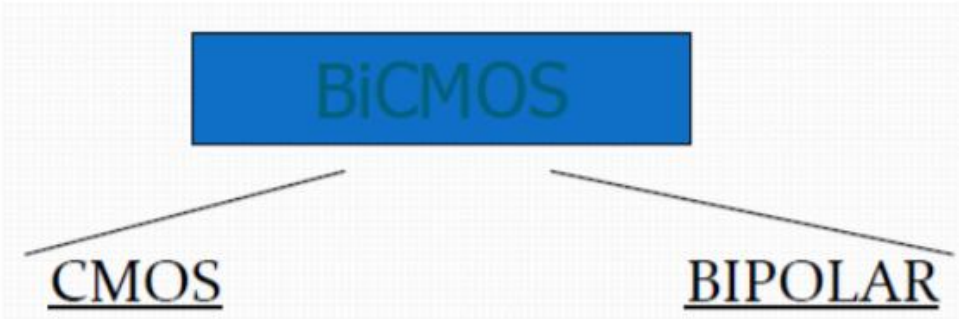
In all other respects-masking, patterning, and diffusion-the process is similar to nMOS fabrication. In summary, typical processing steps are:

- *Mask* 1 - defines the areas in which the deep p-well diffusions are to take place.
- *Mask 2* - defines the thinox regions, namely those areas where the thick oxide is to be stripped and thin oxide grown to accommodate p- and n-transistors and wires.
- *Mask* 3 - used to pattern the polysilicon layer which is deposited after the thin oxide.
- *Mask* 4 - A p-plus mask is now used (to be in effect "Anded" with Mask 2) to define all areas where p-diffusion is to take place.
- *Mask* 5 - This is usually performed using the negative form of the p-plus mask and defines those areas where n-type diffusion is to take place.
- *Mask* 6 - Contact cuts are now defined.
- *Mask* 7 - The metal layer pattern is defined by this mask.

Mask 8 - An overall passivation (overglass) layer is now applied and Mask 8 ts needed to define the openings for access to bonding pads.

Bi-CMOS

Bipolar compatible CMOS(Bi-CMOS) technology:
Introduced in early 1980s
Combines Bipolar and CMOS logic



Low power dissipation
High packing density
High Noise Margin
High input impedance

High speed
High output drive
High transconductance (g_m)

Characteristics of CMOS

Lower static power dissipation

Higher noise margins

Higher packing density

High yield with large integrated complex functions

High input impedance (low drive current)

Scalable threshold voltage

High delay load sensitivity

Low output drive current (issue when driving large capacitive loads)

Bi-directional capability (drain & source are interchangeable)

A near ideal switching device,
Low gain