DIGITAL ELECTRONICS LAB

LABORATORY MANUAL

B.Tech. - EEE

Semester –IV

Subject Code: LC-EE-204G

Name:	
Roll. No.:	
Group/Branch:	

Department of Electrical and Electronics Engineering

DRONACHARYA COLLEGE OF ENGINEERING

Khentawas, Farrukh Nagar (122506), Gurugram, Haryana

Affiliated to MDU University, Rohtak

Table of Contents

1. Vision and Mission of the Institute
2. Vision and Mission of the Department
3. Programme Educational Objectives (PEOs)
4. Programme Outcomes (POs)
5. Programme Specific Outcomes (PSOs)
6. University Syllabus
7. Course Outcomes (COs)
8. CO- PO and CO-PSO mapping
9. Course Overview
10. List of Experiments
11. DOs and DON'Ts
12. General Safety Precautions
13. Guidelines for students for report preparation
14. Lab assessment criteria
15. Details of Conducted Experiments
16. Lab Experiments

Vision and Mission of the Institute

Vision:

"To impart Quality Education, to give an enviable growth to seekers of learning, to groom them as World Class Engineers and Managers competent to match the expanding expectations of the Corporate World has been our ever enlarging vision extending to new horizons since the inception of Dronacharya College of Engineering."

Mission:

M1. To prepare students for full and ethical participation in a diverse society and encourage lifelong learning by following the principle of 'Shiksha evam Sahayata' i.e. Education & Help.

M2. To impart high-quality education, knowledge and technology through rigorous academic programs, cutting-edge research, & Industry collaborations, with a focus on producing engineers& managers who are socially responsible, globally aware, & equipped to address complex challenges.

M3. Educate students in the best practices of the field as well as integrate the latest research into the academics.

M4. Provide quality learning experiences through effective classroom practices, innovative teaching practices and opportunities for meaningful interactions between students and faculty.

M5. To devise and implement programmes of education in technology that are relevant to the changing needs of society, in terms of breadth of diversity and depth of specialization.

Vision and Mission of the Department

Vision:

"Our vision for the Electrical and Electronics Engineering (EEE) Department is to be a globally recognized Centre of excellence in education, research, and innovation in the field of electrical and electronics engineering. We strive to produce competent engineers with strong technical knowledge, ethical values, and a passion for lifelong learning. And also to contribute to the sustainable development of society through cutting-edge research, industry collaborations, and community engagement"

Mission:

M1: To provide a high-quality education that equips students with a strong foundation in electrical and electronics engineering.

M2: To conduct pioneering research in diverse areas of electrical and electronics engineering

M3: To establish strong ties with industry partners to bridge the gap between academia and the professional world.

M4: To instilling ethical values, social responsibility, and environmental consciousness in our students.

M5: To regularly assess and upgrade our teaching methodologies, infrastructure, and facilities

Program Educational Objectives (PEO) of B.Tech, Electrical and Electronics Engineering

PEO1. Engineers will practice the profession of engineering using a systems perspective and analyze, design, develop, optimize & implement engineering solutions and work productively as engineers, including supportive and leadership roles on multidisciplinary teams.

PEO2. Continue their education in leading graduate programs in engineering & interdisciplinary areas to emerge as researchers, experts, educators & entrepreneurs and recognize the need for, and an ability to engage in continuing professional development and life-long learning.

PEO3. Engineers, guided by the principles of sustainable development and global interconnectedness, will understand how engineering projects affect society and the environment.

PEO4. Promote Design, Research, and implementation of products and services in the field of Engineering through Strong Communication and Entrepreneurial Skills.

PEO5. Re-learn and innovate in ever-changing global economic and technological environments of the 21st century.

Programme Outcomes (POs)

PO1. Apply knowledge of computing, mathematical foundations, algorithmic principles, and engineering theory in the modeling and design of systems to real-world problems (fundamental engineering analysis skills).

PO2. Apply and integrate knowledge and understanding of other engineering disciplines to support study of their own engineering discipline.

PO3. Design and conduct experiments, as well as to analyze and interpret data (information retrieval skills).

PO4. Practical application of engineering skills, combining theory and experience, and use of other relevant knowledge and skills.

PO5. Analyze a problem, identify, formulate and use the appropriate computing and engineering requirements for obtaining its solution(engineering problem solving skills).

PO6. Identify, classify and describe the performance of systems and components through the use of analytical methods and modeling techniques.

PO7. Investigate and define a problem and identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues.

PO8. Communicate effectively, both in writing and orally (speaking / writing skills).

PO9. Adapt to a rapidly changing environment by having learned and applied new skills and new technologies.

PO10. To significantly contribute to delivery of desired component, product, or process.

PO11. Formulate and solve moderately complex engineering problems, accounting for hardware/software/human interactions.

PO12. Recognize the importance of professional development by pursuing postgraduate studies or face competitive examinations that offer challenging and rewarding careers in computing.

Program Specific Outcomes (PSOs)

PSO1: Equip themselves to potentially rich & employable field of Engineering. Analyse and design electrical machines, circuits, controls and systems which makes the part of Power generation, transmission, distribution, utilization and conservation

PSO2: Pursue higher studies in the contemporary Technologies and multidisciplinary fields with an inclination towards continuous learning in the area of Power quality, high voltage, power electronics and Renewable energy systems

PSO3: Take up-self- employment in Indian and global software market in designing , implementing and testing analog, digital , embedded and signal processing systems

PSO4: Meet the requirements of the Indian Standards and use knowledge in different domains to identify the research gaps and to provide innovative solutions.

University Syllabus

LIST OF EXPERIMENTS:

1. To study & design basic gates.
2. To realize and minimize five & six variables using K-Map method .
3. To verify the operation of Multiplexer & De-multiplexer.
4. To perform Half adder and Full adder.
5. To perform Half Substractor and Full substractor.
6. To verify the truth table of S-R,J-K,T & D Type flip flop .
7. To study FLIP- FLOP conversion.
8. To design & verify the operation of 3 bit synchronous counter.
9. To design & verify the operation of synchronous UP/DOWN decade counter using JK flip.
10. To design & verify operation of Asynchronous counter.
11. To design and implement a ckt to detect a Count Sequence.
12. Conversion of state diagram to the state table and implement it using logical ckt.

Course Outcomes (COs)

The objectives of this course are as under:

1. To provide a comprehensive introduction to digital logic design leading to the ability to understand binary codes, binary arithmetic and Boolean algebra and its relevance to digital logic design.
2. To design & analyze modular combinational circuits with MUX/DEMUX, Decoder, Encoder etc.
3. To design & analyze synchronous sequential logic circuits.
4. To familiarize students with basics of digital logic families.
5. To Analyze and design simple systems composed of PLDs.

CO-PO Mapping

CO \ PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1		3			2	3	1		1
CO2	1		3	2	3	1			3	1		1
CO3	1	2	3		2		2		3	1		1
CO4	1		3		3			2	3	1		1
CO5	1		1		3			2	3	1		1

CO-PSO Mapping

CO \ PSO	PSO1	PSO2	PSO3	PSO4
CO1	3	2	1	2
CO2	1		3	3
CO3	1	2	3	
CO4	1	3	2	
CO5	1		1	

Course Overview

Digital Electronics Lab is helpful for the students to acquire the basic knowledge of digital logic levels and its application to construct digital electronics circuits. This course will prepare students to perform the analysis and design of various digital electronic circuits. Designing and implementing digital circuits imparts practical knowledge of working with electronics circuits in students. The innovations and ideas bud from a mind that has hands-on experience of hardware integration. This laboratory also helps students develop the real time problem skills which are an important take-away point of troubleshooting the designed circuits.

The following guidelines should be followed regarding award of marks:

Class Work : 25 Marks
Theory : 25Marks
Total : 50 Marks
Duration of Exam. : 3 Hrs.

General instructions: Practical examination to be conducted immediately after the Pre-university examinations covering entire lab experiments given above. Evaluation is a serious process that is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per group should not exceed 5 and in a batch size of not more than 30. Students shall be allowed for the University examination only on submitting the duly certified internal examination record. The external examiner shall endorse the record and conduct the external examination as per guidelines laid by affiliated university.

List of Experiments mapped with Cos

S. No.	NAME OF THE EXPERIMENT	Course Outcome
1.	TO STUDY AND DESIGN BASIC GATES.	CO1
2.	TO REALIZE AND MINIMIZE 5 & 6 VARIABLES USING K-MAP METHOD	CO1, CO2,
3.	TO VERIFY OPERATION OF MULTIPLEXER & DE-MULTIPLEXER.	CO2, CO3
4.	TO DESIGN AND VERIFY OPERATION OF HALF ADDER AND FULL ADDER.	CO1, CO2
5.	TO DESIGN AND VERIFY OPERATION OF HALF & FULL SUBTRACTOR	CO1, CO2
6.	VERIFICATION OF STATE TABLES OF SR, JK, T AND D FLIP-FLOPS USING NAND & NOR GATES.	CO3, CO4
7.	TO STUDY FLIP-FLOP CONVERSION.	CO1,CO4
8.	DESIGN AND VERIFY THE 3-BIT SYNCHRONOUS COUNTER.	CO1, CO2, CO4
9.	TO DESIGN & VERIFY OPERATION OF SYNCHRONOUS UP/DOWN COUNTER USING JK FLIP FLOP.	CO1, CO3, CO4
10.	DESIGN AND VERIFY THE 4-BIT ASYNCHRONOUS COUNTER.	CO4, CO5

DOs and DON'Ts

DO'S	DON' TS
1. **Be regular to the lab.**	1. Do not exceed the voltage Rating.
2. **Follow proper Dress Code.**	2. Do not inter change the IC's while doing the experiment.
3. **Maintain Silence.**	3. Avoid loose connections and short circuits.
4. **Know the theory behind the experiment before coming to the lab.**	4. Do not throw the connecting wires to floor.
5. **Identify the different leads or terminals or pins of the IC before making connection.**	5. Do not come late to the lab.
6. **Know the Biasing Voltage required for different families of IC's and connect the power supply voltage and ground terminals to the respective pins of the IC's.**	6. Do not operate μp/IC trainer kits unnecessarily.
7. **Know the Current and Voltage rating of the IC's before using them in the experiment.**	7. Do not panic if you don't get the output.
8. **Avoid unnecessary talking while doing the experiment.**	
9. **Handle the IC Trainer Kit properly.**	

General Safety Precautions

Precautions (In case of Injury or Electric Shock)

1. To break the victim with live electric source, use an insulator such as fire wood or plastic to break the contact. Do not touch the victim with bare hands to avoid the risk of electrifying yourself.
2. Unplug the risk of faulty equipment. If main circuit breaker is accessible, turn the circuit off.
3. If the victim is unconscious, start resuscitation immediately, use your hands to press the chest in and out to continue breathing function. Use mouth-to-mouth resuscitation if necessary.
4. Immediately call medical emergency and security. Remember! Time is critical; be best.

Precautions (In case of Fire)

1. Turn the equipment off. If power switch is not immediately accessible, take plug off.
2. If fire continues, try to curb the fire, if possible, by using the fire extinguisher or by covering it with a heavy cloth if possible isolate the burning equipment from the other surrounding equipment.
3. Sound the fire alarm by activating the nearest alarm switch located in the hallway.
4. Call security and emergency dept. immediately:

Emergency : Reception

Security : Main Gate

Guidelines to students for report preparation

All students are required to maintain a record of the experiments conducted by them. Guidelinesfor its preparation are as follows: -

1) All files must contain a title page followed by an index page. ***The files will not be signed by thefaculty without an entry in the index page.***

2) Student's Name, Roll number and date of conduction of experiment must be written on allpages.

3) For each experiment, the record must contain the following

(i) Aim/Objective of the experiment
(ii) Pre-experiment work (as given by the faculty)
(iii) Lab assignment questions and their solutions
(iv) Test Cases (if applicable to the course)
(v) Results/ output

Note:

1. Students must bring their lab record along with them whenever they come for the lab.
2. Students must ensure that their lab record is regularly evaluated.

Lab Assessment Criteria

An estimated 10 lab classes are conducted in a semester for each lab course. These lab classes are assessed continuously. Each lab experiment is evaluated based on 5 assessment criteria as shown in following table. Assessed performance in each experiment is used to compute CO attainment aswell as internal marks in the lab course.

Grading Criteria	**Exemplary (4)**	**Competent (3)**	**Needs Improvement (2)**	**Poor (1)**
AC1: Pre-Lab written work(this may be assessed through viva)	Complete procedure with underlined concept is properly written	Underlined concept is written but procedureis incomplete	Not able to write concept and procedure	Underlined concept is not clearly understood
AC2: Program Writing/ Circuit connection	Assigned problem is properly analyzed, correct solution designed, appropriate language constructs/ tools are applied, Program/solution written is readable	Assigned problem is properly analyzed, correct solution designed, appropriate language constructs/ tools are applied	Assigned problem is properly analyzed & correct solution designed	Assigned problem is properly analyzed
AC3: Identification & Removal of Error / Troubleshooting	Able to identify errors/hardwiring and remove them	Able to identify errors/ circuit based errors and remove themwith little bit of guidance	Is dependent totally on someone for identification of errors and their removal	Unable to understand the reason for errors even after they are explicitly pointed out
AC4:Executi on & Demonstrationn	All variants of input /output are tested, Solution is well demonstrated and implemented concept is clearly explained	All variants of input /output are not tested, However, solution is well demonstrated and implemented concept is clearly explained	Only few variants of input /output are tested, Solution is well demonstrated but implemented concept is not clearly explained	Solution is not well demonstrated and implemented concept is not clearly explained
AC5:Lab Record Assessment	All assigned problems are well recorded with objective, design constructs and solution along with Performance analysis using all variants of input and output	More than 70 % of the assigned problems are well recorded with objective, design contracts and solution along with Performance analysis is done with all variants of input and output	Less than 70 % of the assigned problems are well recorded with objective, design contracts and solution along with Performance analysis is done with all variants of input and output	Less than 40 % of the assigned problems are well recorded with objective, design contracts and solution along with Performance analysis is done with all variants of input and output

LAB EXPERIMENTS

EXPERIMENT No. 1

Aim: - **To study and design basic gates.**

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, IC's (7400, 7402, 7404, 7408, 7432, and 7486)

THEORY:

AND Gate: The AND operation is defined as the output as (1) one if and only if all the inputs are (1) one. 7408 is the two Inputs AND gate IC.A&B are the Input terminals &Y is the Output terminal.

$$Y = A.B$$

OR Gate: The OR operation is defined as the output as (1) one if one or more than 0 inputs are (1) one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

$$Y = A + B$$

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

$Y = A$ NOT B, $Y = A'$

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

$$Y = (A.\ B)'$$

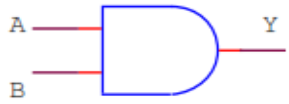
NOR GATE: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate.

$$Y = (A+B)'$$

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two inputs IC. EX-OR gate is not a basic operation & can be performed using basic gates.

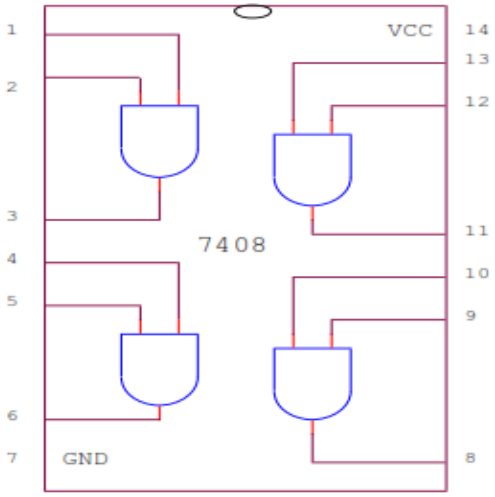
$$Y = A \oplus B$$

AND GATE (7408)

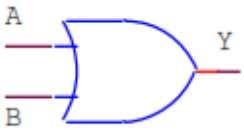


Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

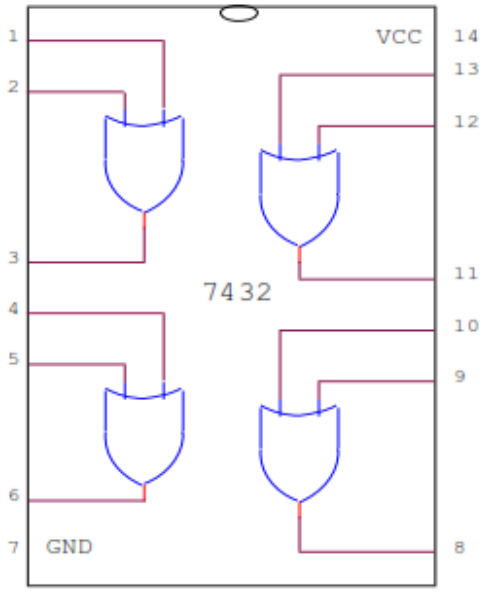


OR GATE (7432)

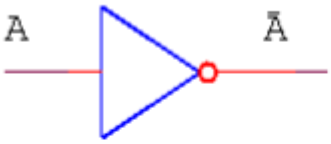


Truth Table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

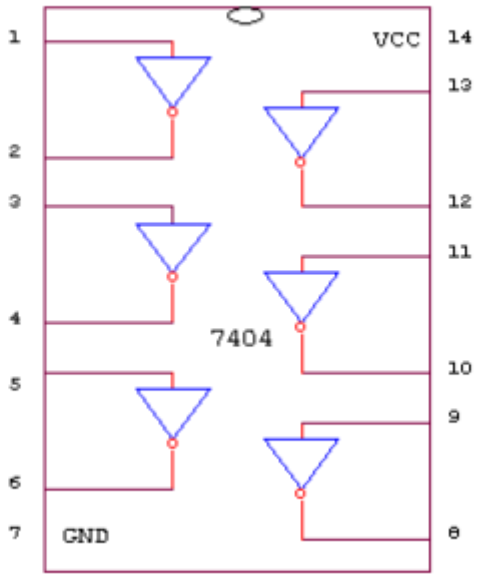


NOT GATE (7404)

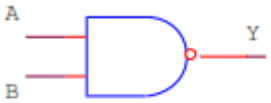


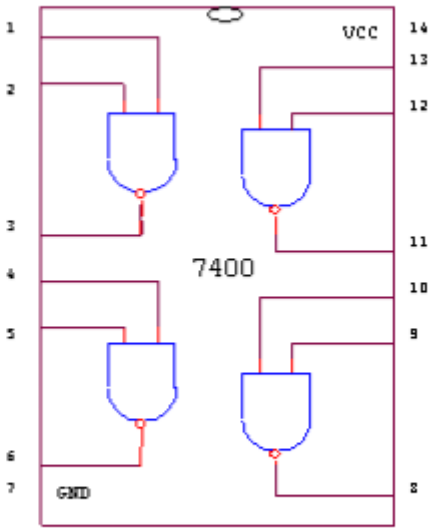
Truth Table

A	Y=Ā
0	1
1	0



NAND GATE (7400)

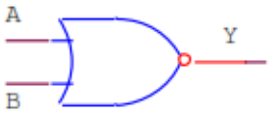


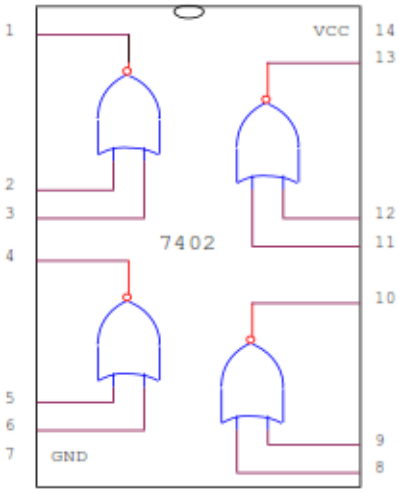


Truth Table

A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE (7402)

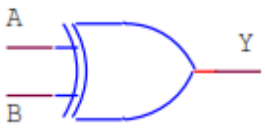




Truth Table

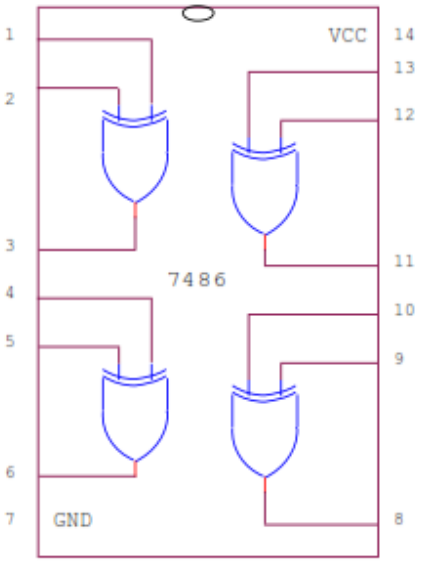
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

EX-OR GATE (7486)



Truth Table

A	B	Y=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0



PROCEDURE:

(a) Fix the IC's on b readboard & give the s upply.
(b) Con nect the +ve terminal of supply to pin 14 & -ve to pin 7.
(c) Give input at pin 1, 2 & tak e output fro m pin 3. It i s same for all e xcept NOT & NOR IC.
(d) For NOR, pin 1 is output & pin 2&3 are inputs.
(e) For NOT, pin 1 is input & p in 2 is output.
(f) Note the values of output fo r different combination of inputs & draw the TRU TH TABLE .

OBSERVATIO N TABLE:

INP UTS		OUTP UTS					
A	B	A' NOT	A+B OR	(A+B)' NOR	(A *B) A ND	(A*B)' NAND	(A⊕B) Ex-OR
0	0	1	0	1	0	1	0
0	1	1	1	0	0	1	1
1	0	0	1	0	0	1	1
1	1	0	1	0	1	0	0

RESULT: We have learnt all the gates ICs accordin g to the IC p in diagram.

PRECAUTIONS:

1. Make the connection s according to the IC pin diagram.

2. The connections shou ld be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Define gates ?
Ans. Gates are the digital circuits, which perform a specific type of logical operation.
Q.2 Complement of the expression A'B + CD' is
Ans. (A + B')(C' + D)
Q.3 Explain Demorgan's theorem.
Ans. (AB)'=A'+B'
(A+B)'=A'.B'
Q.4 (A+A) A =?
Ans. A.
Q5 Binary subtraction of 101101 – 001011 =?
Ans. 100010
Q6. What is the addition of the binary numbers 11011011010 and 010100101?
Ans. 11101111111
Q7 The decimal number 10 is represented in its BCD form as
Ans. The decimal number 10 is represented in its BCD form as 0001 0000, in accordance to 8421 for each of the two digits.
Q8. The excess-3 code for 597 is given by
Ans. The addition of '3' to each digit yields the three new digits '8', '12' and '10'. Hence, the corresponding four-bit binary equivalents are 100011001010, in accordance to 8421 format.
Q9. The given hexadecimal number (1E.53)16 is equivalent to
Ans. (1E.53)16 = (0001 1110.0101 0011)2
= (00011110.01010011)2
= (011110.010100110)2
= (011 110.010 100 110)2
= (36.246)8
Q10. Convert binary to octal: $(110110001010)_2$ =?
Ans. The binary equivalent is segregated into groups of 3 bits, starting from left. And then for each group, the respective digit is written. Thus, the octal equivalent is obtained. (110110001010)2 = (6612)8

EXPERIMENT No. 2

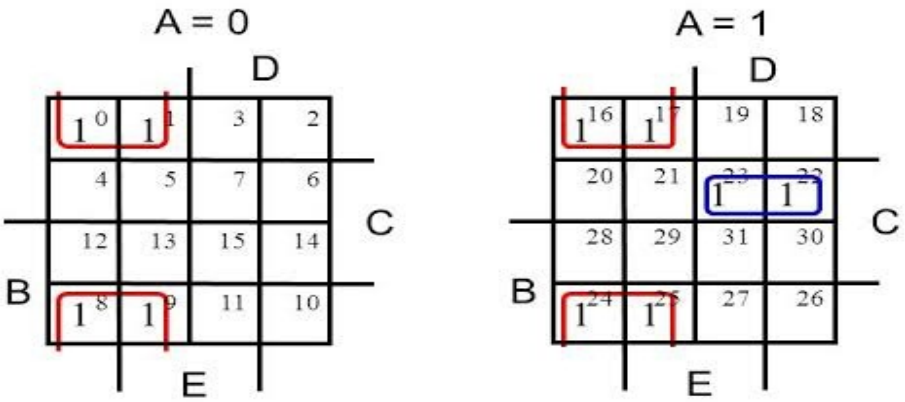
Aim: To realize and minimize 5 & 6 variables using K-Map Method

THEORY:

A Karnaugh map (K-map) is a pictorial method used to minimize Boolean expressions without having to use Boolean algebra theorems and equation manipulations. A K-map can be thought of as a special version of a truth table. Using a K-map, expressions with two to four variables are easily minimized. Canonical Forms (Normal Forms): Any Boolean function can be written in disjunctive normal form (sum of min-terms) or conjunctive normal form (product of max-terms). A Boolean function can be represented by a Karnaugh map in which each cell corresponds to a minterm. The cells are arranged in such a way that any two immediately adjacent cells correspond to two minterms of distance 1. There is more than one way to construct a map with this property.

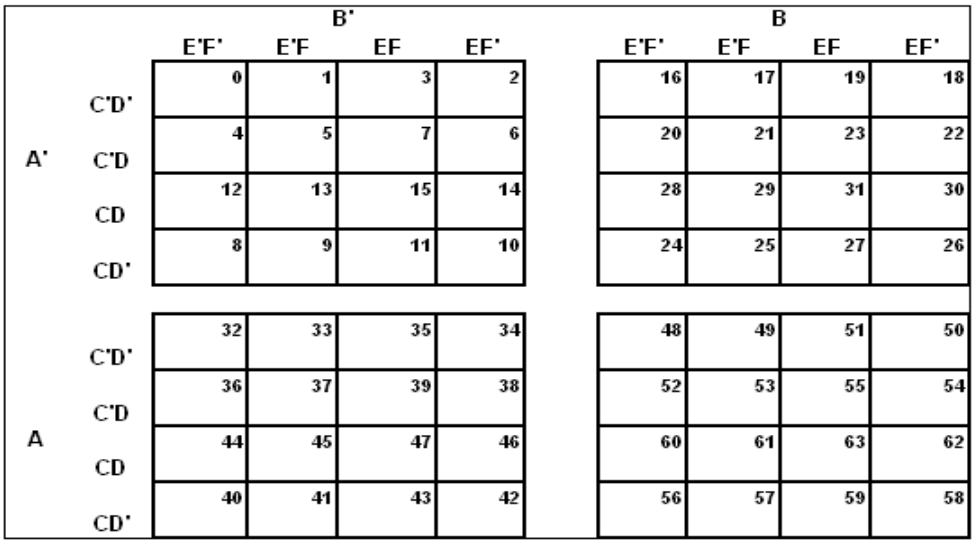
Example of a Five-Variable K-map

- $F(A, B, C, D, E) = \sum(0, 1, 8, 9, 16, 17, 22, 23, 24, 25)$
- $F = \overline{C}\,\overline{D} + A\,\overline{B}\,C\,D$



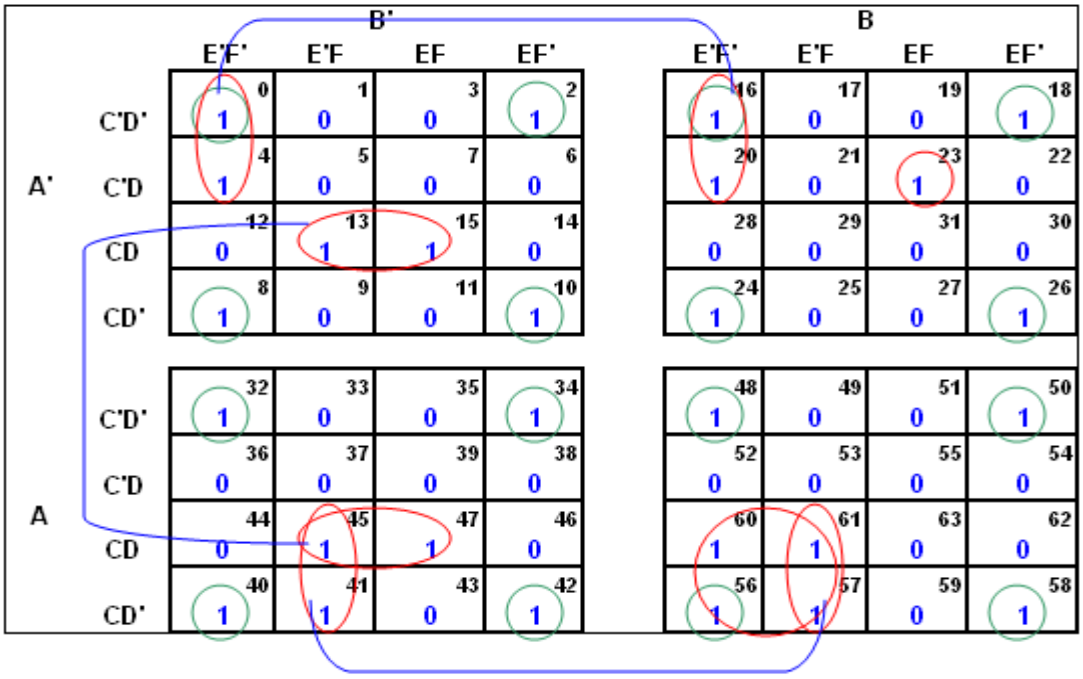
6-Variable K-Map

A 6-variable K-Map is drawn as below:



Given function, **F = Σ (0, 2, 4, 8, 10, 13, 15, 16, 18, 20, 23, 24, 26, 32, 34, 40, 41, 42, 45, 47, 48, 50, 56, 57, 58, 60, 61)**

Let's draw K-Map for this function by writing 1 in cells that are present in function and 0 in rest of the cells.



Applying rules of simplifying K-Map, there is one loop which has 16 1′s – containing 1′s at all the corners of all 4 squares. We obtain it by visualizing all the 4 squares over one another but only in horizontal or vertical direction (not diagonal) and figuring out adjacent cells. All the 1′s in corners are circled in green.

There are 4 pairs, one in fourth square at bottom-right and other 3 are between the squares and are highlighted by blue connecting line.

(0, 2, 8, 10, 16, 18, 24, 26, 32, 34, 40, 42, 48, 50, 56, 58) – D'F' (A, B, C and E are changing variables, so they are eliminated)

(41, 45, 57, 61) – ACE'F (B & D are changing variables, so they are eliminated)

(13, 15, 45, 47) – B'CDF (A & E are changing variables, so they are eliminated)

(0, 4, 16, 20) – A'C'E'F' (B & D are changing variables, so they are eliminated)

(56, 57, 60, 61) – ABCE' (D and F are changing variables, so they are eliminated)

There is 1 in cell 23, which cannot be looped with any adjacent cell, hence it cannot be simplified further and left as it is.

23 = A'BC'DEF

Thus, **F = D'F' + ACE'F + B'CDF + A'C'E'F' + ABCE' + A'BC'DEF**

Quiz Questions with answer.

Q.1 Define K-map ?
Ans.It is a method of simplifying Boolean Functions in a systematic mathematical way.
Q.2 Define SOP ?
Ans.Sum of Product.
Q.3 Define POS ?
Ans.Product of Sum.
Q.4 What are combinational circuits?
Ans. These are those circuits whose output depends upon the inputs present at that instant of time.
Q.5 What are sequential circuits?
Ans. These are those circuits whose output depends upon the input present at that time as well as the previous output.
Q.6 The code where all successive numbers differ from their preceding number by single bit is
Ans.The code where all successive numbers differ from their preceding number by single bit is gray code. It is an unweighted code. The most important characteristic of this code is that only a single bit change occurs when going from one code number to next.
Q.7 How many two-input AND and OR gates are required to realize Y = CD+EF+G?
Ans. 2, 2
Q.8 Which code is used for the identification of cells?
Ans8. Gray Code.
Q.9 The following switching functions are to be implemented using a decoder: f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7) The minimum configuration of decoder will be _____
Ans. 4 to 16 line decoder as the minterms are ranging from 1 to 14.
Q.10 When simplified with Boolean Algebra (x + y)(x + z) simplifies to
Ans. x + yz

EXPERIMENT No. 3

Aim: To verify operation of multiplexer & De-multiplexer.

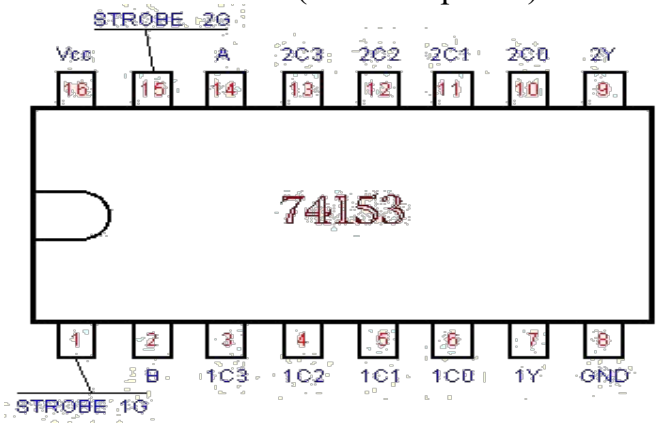
APPARATUS REQUIRED: Power Supply, Digital Trainer, Connecting Leads, IC's 74153(4x1 multiplexer).

BRIEF THEORY:

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output .The fig. (1) Shows the general idea. The circuit has n-input signal, control signal & one output signal. Where 2^n =m. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

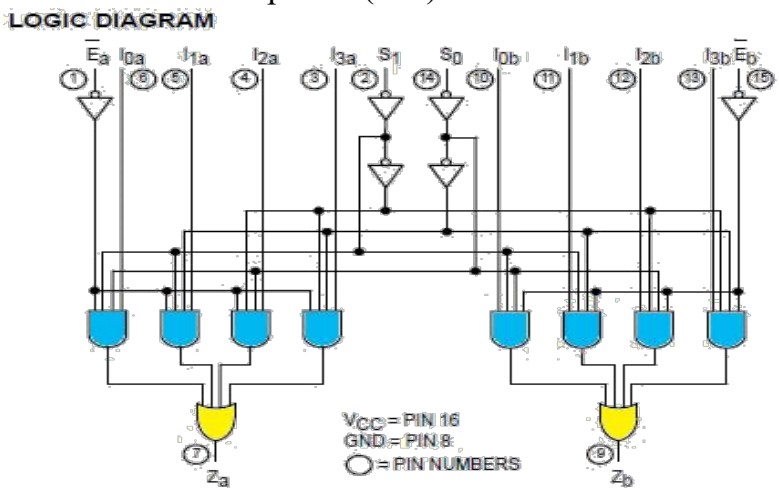
PIN CONFIGURATION;–

IC 74153 (4x1 multiplexer)

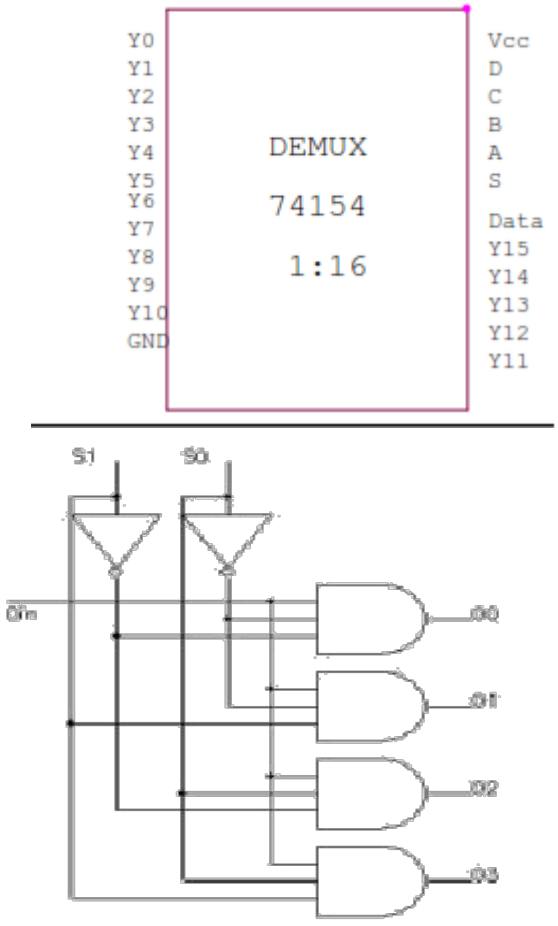


LOGIC DIAGRAM:

Multiplexer (4x1) IC 74153



DEMULTIPLEXER: De-multiplexer means generally one into many. A de-multiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The fig.(2) shows the general idea. The circuit has one input signal, m control signal and n output signals. Where 2 = n. One of the popular de-multiplexer is the 1 to 04 de-multiplexer, Which has 1 input bit, 4 control bits and 16 output bits.



Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

PROCEDURE:

1. Fix the IC's on the bread board &give the input supply.
2. Make connection according to the circuit.
3. Give select signal and strobe signal at respective pins.
4. Connect +5 vVcc supply at pin no 24 & GND at pin no 12.
5. Verify the truth table for various inputs.

OBSERVATION TABLE:

Truth Table of multiplexer (4x1) IC 74153

INPUT							OUTPUT
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

RESULT: Verify the truth table of multiplexer for various inputs.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q. 1 What do you understand by decoder?
Ans.A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the circuit operation.
Q. 2 What is de-multiplexer?
Ans. The de-multiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. It has 2^n outputs. The address input determine which data output is going to have the same value as the data input. The other data outputs will have the value 0.
Q. 3 What do you understand by encoder?
Ans. An encoder or multiplexer is therefore a digital IC that outputs a digital code based on which of its several digital inputs is enabled.
Q. 4 What is the main difference between decoder and de-multiplexer?
Ans. In decoder we have n input lines as in de-multiplexer we have n select lines.
Q. 5 Why Binary is different from Gray code?
Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.
Q. 6 Write down the method of Binary to Gray conversion.
R. Ans. Using the Ex-Or gates.
Q. 7 Convert 0101 to Decimal**.**
Ans. 5
Q. 8 Write the full form of ASCII Codes?
Ans. American Standard Code for Information Interchange.
Q.9. If a register containing 0.110011 is logically added to register containing 0.101010 what would be the result?
Ans.111011
Q10. Why is a de-multiplexer called a data distributor?
Ans. A de-multiplexer sends a single input to multiple outputs, depending on the select lines. For one input, the de-multiplexer gives several outputs. That is why it is called a data distributor.

EXPERIMENT NO: 4

Aim: To design and verify operation of half adder and full adder.

APPARATUS REQUIRED: Power supply, IC's, Digital Trainer, Connecting leads.

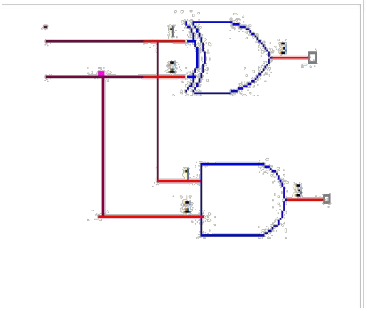
BRIEF THEORY: We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

Half Adder: It is a logic circuit that adds two bits. It produces the O/P, sum & carry.
Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

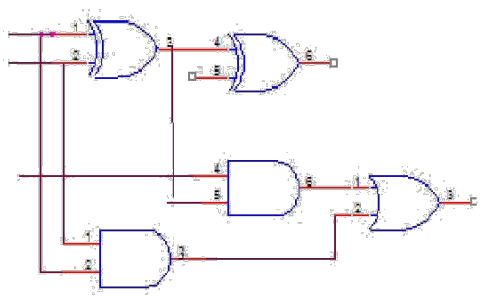
Full Adder: It is a logic circuit that can add three bits. It produces two O/P sum & carry.
Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

LOGIC DAIGRAM:

Half Adder



Full Adder

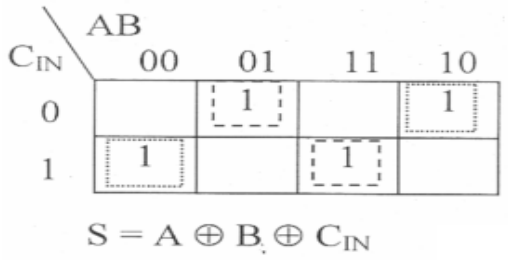


PROCEDURE:

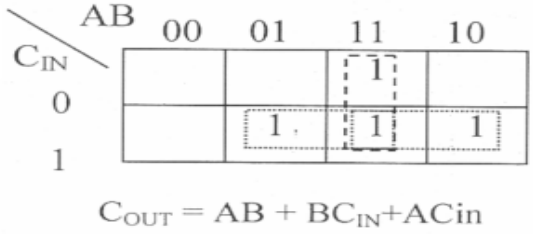
(a) Connect the ckt. as shown in fig. For half adder.
(b) Apply diff. Combination of inputs to the I/P terminal.
(c) Note O/P for Half adder.
(d) Repeat procedure for Full wave.
(e) The result should be in accordance with truth table.

OBSERVATION TABLE:

Logic expressions:



$S = A \oplus B \oplus C_{IN}$



$C_{OUT} = AB + BC_{IN} + ACin$

HALF ADDER:

INPUTS		OUTPUT	
A	**B**	**S**	**C**
0	**0**	**0**	**0**
0	**1**	**1**	**0**
1	**0**	**1**	**0**
1	**1**	**0**	**1**

FULL ADDER:

INPUTS			OUTPUTS	
A	**B**	**C**	**S**	**CARRY**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**

RESULT: The Half Adder & Full Adder ckts. are verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Give the basic rules for binary addition? Ans. 0+0 = 0; 0+1 = 1; 1+1 = 1 0 ; 1+0 = 1.

Q.2 Specify the no. of I/P and O/P of Half adder?

Ans2. Two inputs & one output.

Q.3 What is the drawback of half adder?

Ans. We can't add carry bit from previous stage.

Q.4 Write the equation for sum & carry of half adder?
Ans. Sum = A XOR B; carry = A.B.
Q.5 Write the equation for sum & carry of full adder?
Ans. SUM= A'B'C+A'BC'+AB'C'+ABC; CARRY=AB+BC+AC.
Q.6 How many half adders will be required for Implementing full adder?
Ans. Two half adders and a OR gate.
Q7 Define Bit?
Ans. Bit is an abbreviation for binary digit.
Q8.What is the difference b/w half adder& half sub tractor?
Ans. Half adder can add two bits & half sub tractor can subtract two bits.
Q9. Half subtractor logic circuit has one extra logic element. Name the element?
Ans. Inverter.
Q10. Define Nibble?
Ans. Combination of four bits.

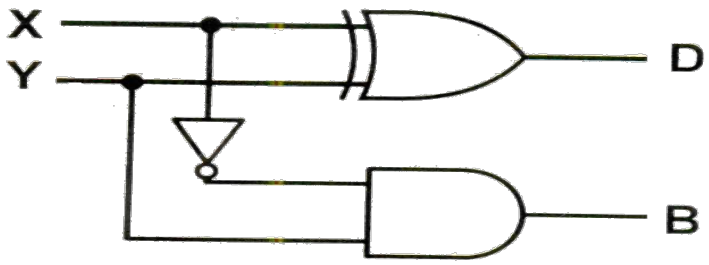
EXPERIMENT NO: 5

Aim: To design and verify operation of half & full Subtractor.

APPARATUS REQUIRED: Digital trainer kit,
IC 7486 (EX-OR)
IC 7408 (AND gate)
IC 7404 (NOT gate)

BRIEF THEORY: A logic circuit for the subtraction of B(subtrahend) from A (minuend) where A& B are 1 bit numbers is referred as half- sub tractor.

LOGIC DIAGRAM :



TRUTH TABLE:

INPUT 1 (X)	INPUT 2 (Y)	BORROW (B)	DIFFERENCE (D)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

PROCEDURE:

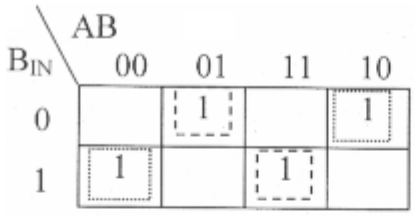
1. Make the connections as per the logic diagram.
2. Connect +5v to pin 14 & ground to pin 7.
3. Apply 0 to input X & Y as per the truth table.
4. Switch on the instrument.
5. Observe the reading on 8 bits LED display.
6. Repeat steps 3 & 5 for different input as per truth table.
7. Verify the truth table.

RESULT: Half sub tractor circuit is studied and verified.

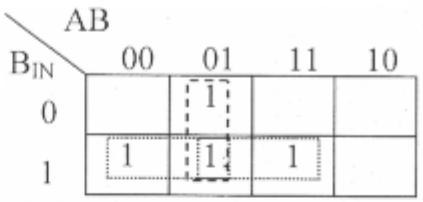
Full Subtractor:

INPUTS			OUTPUTS	
A	B	B_{IN}	D (Difference)	B_{OUT} (Borrow)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Expressions:

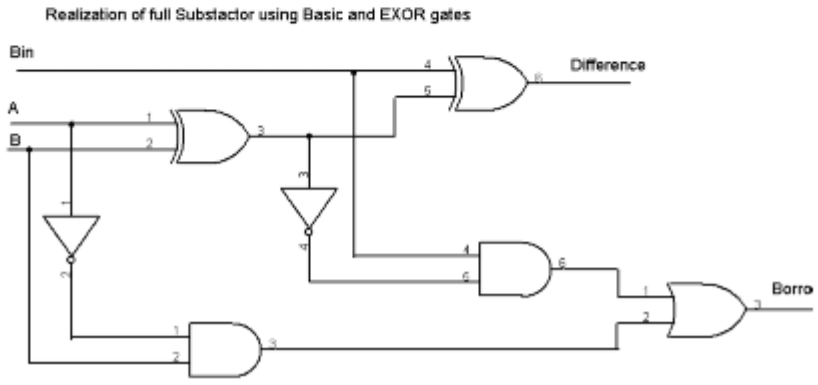


$D = A \oplus B \oplus B_{IN}$



$B_{OUT} = A'B + A'B_{IN} + BinB$

LOGIC DIAGRAM:



RESULT:

Thus the Logic circuit of Full Subtractor Circuit was constructed and the truth table was verified.

Quiz Questions with answer.

Q.1 What is half subs tractor?
Ans. Performs subs traction of two bits.
Q.2 For implementing half subs tractor how many EX-OR, AND gates and Not gates are required?
Ans. One EX-OR, one –AND gate, one- Not gate.
Q.3 What are the logical equations for difference & borrow?
Ans. $D = \bar{A}B + A\bar{B}$
$B = \bar{A}.B$
Q.4 How full subtractor is different from half subs tractor.
Ans. Full sub tractor performs subtraction of three bits but half subs tractor Performs subtraction of two bits.
Q5 If inputs of half subs tractor are A=0, and B=1 then Borrow will be?
Ans. B=1
Q.6 Is 2's complement method appropriate for subtraction?
Ans. 2's complement method is appropriate method for subtraction.
Q.7 How many bits we use in half subtractor for subtraction?
Ans. only two bits.
Q.8Can we use parallel adder for subtraction?
Ans. We can use parallel adder using 2's complement method.
Q.9 Which one is better subtractor or parallel adder for subtraction?
Ans. Parallel adder is the best option using 1's complement or 2's complement
Q.10 Which adder is used for addition of BCD numbers?
Ans. BCD adder.

EXPERIMENT NO: 6

Aim: Verification of state tables of SR, JK, T and D flip-flops using NAND & nor gates.

APPARATUS REQUIRED:IC' S 7400, 7402 Digital Trainer & Connecting leads.

BRIEF THEORY:

- **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

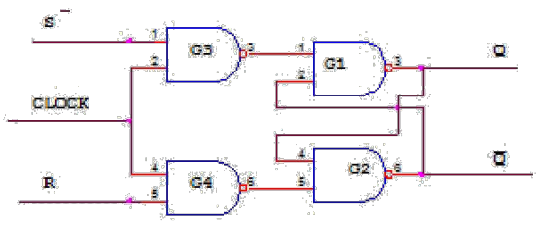
- **JK FLIP-FLOP**: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

- **D FLIP –FLOP**: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

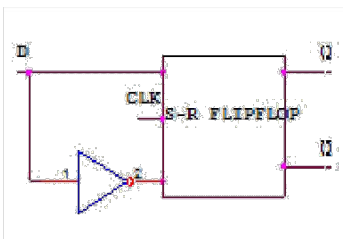
- **T FLIP-FLOP**: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

CIRCUIT DIAGRAM:

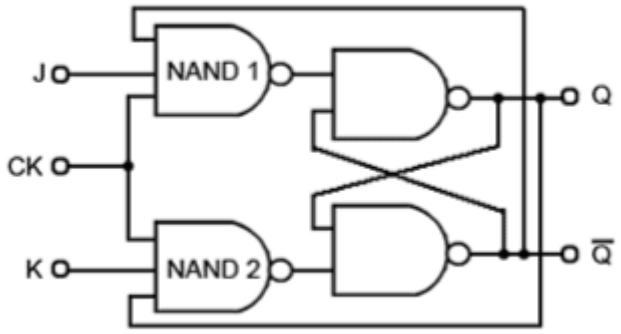
SR Flip Flop



D Flip Flop



JK Flip Flop



TRUTH TABLE:
SR F LIP FLOP:

CLOCK	S	R	Q_{n+1}
1	0	0	NO CH ANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FL IPFLOP:

INPUT	OU TPUT
0	0
1	1

JK FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	0	NO CH ANGE
1	0	1	0
1	1	0	1
1	1	1	Qn ’

T FL IPFLOP

CLOCK	S	R	Q_{n+1}
1	0	1	NO CH ANGE
1	1	0	Qn ’

RESULT: Truth table is verified on digital trainer.

Quiz Questions with answer.

Q 1.Flip flop is Astable or Bistable?
Ans. Bistable.
Q2.What are the I/Ps of JK flip–flop where this race round condition occurs?
Ans. Both the inputs are 1.
Q3.When RS flip-flop is said to be in a SET state?
Ans.When the output is 1.
Q4.When RS flip-flop is said to be in a RESET state?
Ans.When the output is 0.
Q5.What is the truth table of JK flip-flop?

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n,

EXPERIMENT NO: 7

Aim: To study Flip-Flop Conversion.

Theory: For the conversion of one **flip flop** to another, a combinational circuit has to be designed first. If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. Thus, the output of the actual flip flop is the output of the required flip flop.

- **SR Flip Flop to JK Flip Flop**

As told earlier, J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.

The truth tables for the flip flop conversion are given below. The present state is represented by Qp and Qp+1 is the next state to be obtained when the J and K inputs are applied.

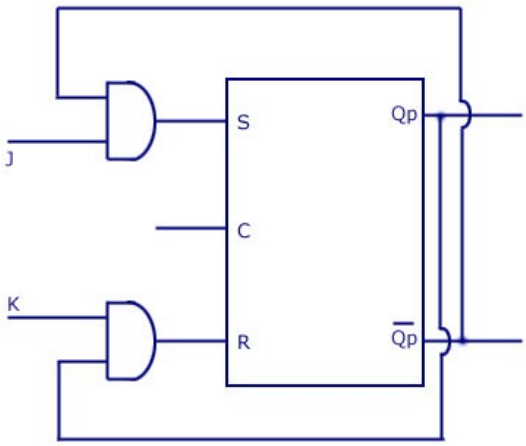
For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Qp, the corresponding Qp+1 states are found. Qp+1 simply suggests the future values to be obtained by the JK flip flop after the value of Qp. The table is then completed by writing the values of S and R required to get each Qp+1 from the corresponding Qp. That is, the values of S and R that are required to change the state of the flip flop from Qp to Qp+1 are written.

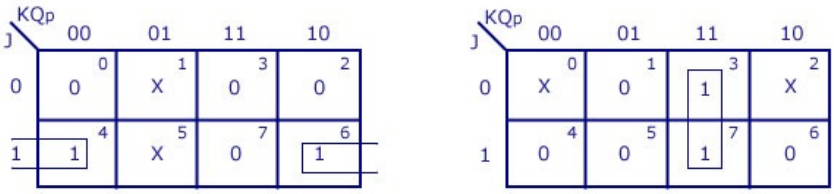
S-R Flip Flop to J-K Flip Flop

Conversion Table

J-K Inputs		Outputs		S-R Inputs	
J	K	Qp	Qp+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Logic Diagram





K-Map

SR Flip Flop to JK Flip Flop

- **JK Flip Flop to SR Flip Flop**

This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Qp. The logic diagram is shown below.

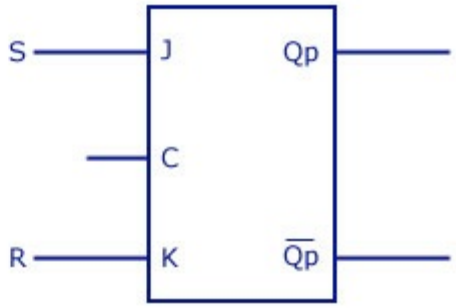
A conversion table is to be written using S, R, Qp, Qp+1, J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Qp+1 outputs are found ut. The outputs for the combinations of S=1 and R=1 are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as “don’t cares”.

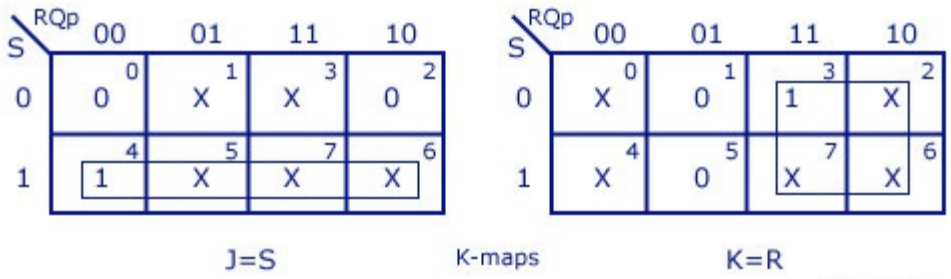
J-K Flip Flop to S-R Flip Flop

Conversion Table

S-R Inputs		Outputs		J-K Inputs	
S	R	Qp	Qp+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

Logic Diagram





JK Flip Flop to SR Flip Flop

Quiz Questions with answer.

Q1.What is the function of clock signal in flip-flop?
Ans. To get the output at known time.
Q2.What is the advantage of JK flip-flop over RS flip-flop?
Ans. In RS flip-flop when both the inputs are 1 output is undetermined.
Q3.In D flip-flop I/P = 0 what is O/P?
Ans.0
Q4.In D flip-flop I/P = 1 what is O/P?
Ans.1
Q5.In T flip-flop I/P = 1 what is O/P?
Ans.0.

EXPERIMENT NO: 8

Aim: Design, and Verify the 3-Bit Synchronous Counter

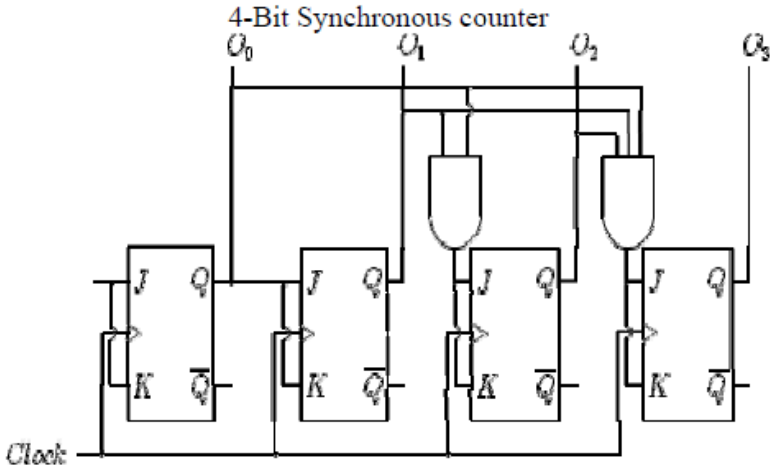
APPARATUS REQUIRED: Digital trainer kit and 3 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEFTHEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

PIN CONFIGURATION:

Dual JK Master Slave Flip Flop with clear and preset

Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input



7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

OBSERVATIONTABLE:

Truth Table

States				Count
0_4	0_3	0_2	0_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT:3-bit synchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 What do you understand by counter?
Ans. Counter is a register which counts the sequence in binary form.
Q.2What is asynchronous counter?
Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.
Q.3What is synchronous counter?
Ans. Where Clock input is common to all FF.
Q.4Which flip flop is used in asynchronous counter?
Ans. All Flip-Flops are toggling FF.
Q.5Which flip flop is used in synchronous counter?
Ans. Any FF can be used.
Q.6 What do you understand by modulus?
Ans.The total no. of states in counter is called as modulus.If counter is modulus-n, then it has n different states.
Q.7 Whatdo you understand by state diagram?
Ans. State diagram of counter is a pictorial representation of counter states directed by arrows in graph.
Q.8 What do you understand by up/down counter?
Ans.Up/Down Synchronous Counter: two way counter which able to count up or down.
Q.9 Why Asynchronous counter is known as ripple counter?
Ans. Asynchronous Counter: flip-flop doesn't change condition simultaneously because it doesn't use single clock signalAlso known as ripple counter because clock signal input as ripple through counter.
Q.10 which type of counter is used in traffic signal?
Ans. Down counters.

EXPERIMENT NO: 9

Aim: To design & Verify operation of synchronous UP/Down counter using JK Flip flop.

Step1:

Construst the state table as below:

Present State	Next State
111	110
110	101
101	100
100	011
011	010
010	001
001	000
000	111

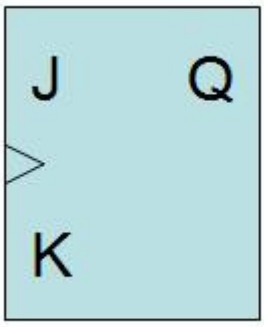
State Table

It is clearly that the count-down function has 8 states. In other words, the design is a MOD-8 counter.

This state table does not follow the sequence from low (000) to high (111) but it does follow with the description function of count-down function. It might lead to mistakes when constructing Kmap.

Step2:

Construct JK excitation table since JK flip-flops are used in this design:



JK Flip-Flop

In order to do that, the characteristic of JK flip-flop must be completely comprehended. The diagram below shows the JK flip-flop characteristic, which has 4 modes.

J	K	Next State (Q_{n+1})	Mode
0	0	Q_n	Holding
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q_n}$	Toggle

JK Flip Flip Characteristic Table

JK flip-flop is in holding mode and toggle mode when the JK inputs are 00 and 11 respectively. If JK inputs are 01, JK flip-flop is in reset mode, while the inputs are 10, JK flip-flop is in set mode. It behaves almost like SR flip-flop but JK flip-flop has toggle mode.

Present State (Q_n)	Next State (Q_{n+1})	J	K	Mode
0	0	0	d	Holding
0	1	1	d	Set
1	0	d	1	Reset
1	1	d	0	Toggle

Excitation Table

You must know how to translate JK characteristic table to JK excitatation table as shown in the table above. It is very crucial to start a design with JK flip-flops.

In what condition, the first row of excitation table 0-->0 is met? By refering to JK charateristic table, the condition can be fulfilled by first and second rows of characteristic table, which JK inputs are 00 and 01. Hence, the J input must be "0" and K input must be "d" (don't care) in the excitation table.

Applying the same concept, JK inputs are "1""d" for the transition from 0 to 1 because of row 3 & 4 of JK characteristic table. (row 4=toggling mode)

JK inputs are "d""1" for the transition from 1 to 0 because of row 2 & 4 of JK characteristic table.
JK inputs are "d""0" for the transition from 1 to 1 because of row 1 & 3 of JK characteristic table.

Step3:
Construct the state table with corresponding excitation table:

With the information from JK excitation table, the state table with corresponding excitation table can be constructed as shown in the first diagram.

Present State	Next State	J_2K_2	J_1K_1	J_0K_0
111	110	d 0	d 0	d 1
110	101	d 0	d 1	1 d
101	100	d 0	0 d	d 1
100	011	d 1	1 d	1 d
011	010	0 d	d 0	d 1
010	001	0 d	d 1	1 d
001	000	0 d	0 d	d 1
000	111	1 d	1 d	1 d

State Table and Corresponding Excitation Table (d=don't care)

NOTE: state table only states out the transition from present state to next state without corresponding excitation table. In short, it consists of the first and second columns of the above diagram.

Step4:

Build Karnaugh Map or Kmap for each JK inputs:

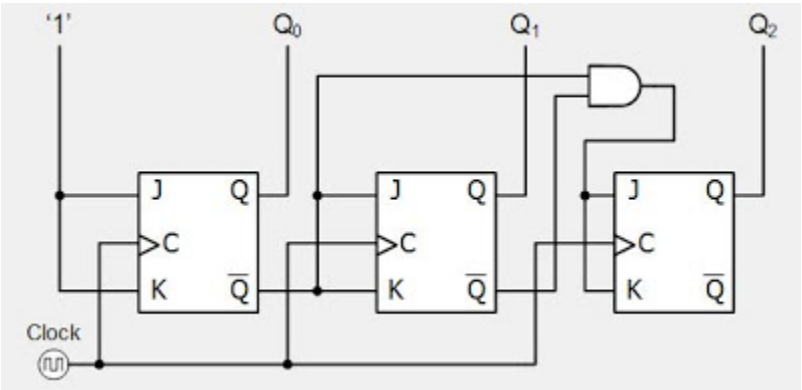
It will be wise if the present state of the state table follows correct sequence from low (000) to high (111) as the diagram below to avoid silly mistakes happen when transfering from state table with corresponding excitation table to the Kmap. Mistakes do happen!!

Present State	Next State	J_2K_2	J_1K_1	J_0K_0
000	111	1 d	1 d	1 d
001	000	0 d	0 d	d 1
010	001	0 d	d 1	1 d
011	010	0 d	d 0	d 1
100	011	d 1	1 d	1 d
101	100	d 0	0 d	d 1
110	101	d 0	d 1	1 d
111	110	d 0	d 0	d 1

state table with correct sequence

Step5:

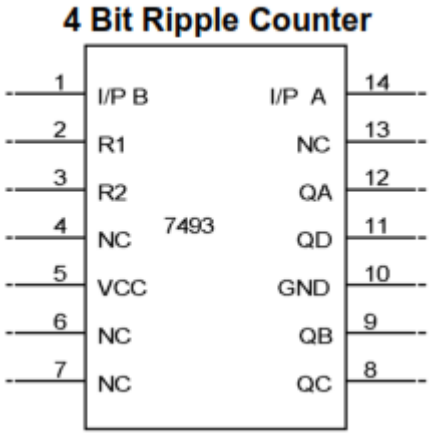
Draw the complete design as below:



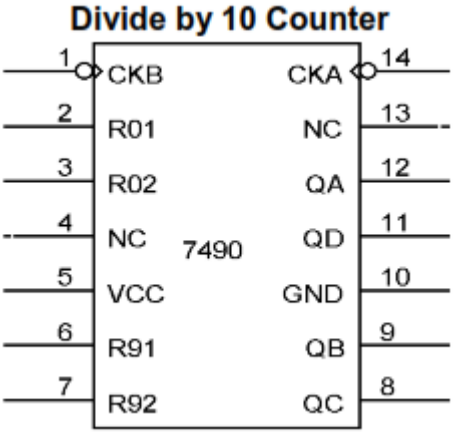
3-bit synchronous down counter with JK flip-flop circuit

Quiz Questions with answer.

Q.1 What do you understand by up/down counter?
Ans. Up/Down Synchronous Counter: two way counter which able to count up or down.
Q.2 Why Asynchronous counter is known as ripple counter?
Ans. Asynchronous Counter: flip-flop doesn't change condition simultaneously because it doesn't use single clock signal Also known as ripple counter because clock signal input as ripple through counter.
Q.3 which type of counter is used in traffic signal? Ans. Down
counters.
Q.4 Draw pin diagram of 4 bit ripple Counter.



Q.5 Draw pin diagram of Divide by 10 Counter.



EXPERIMENT NO: 10

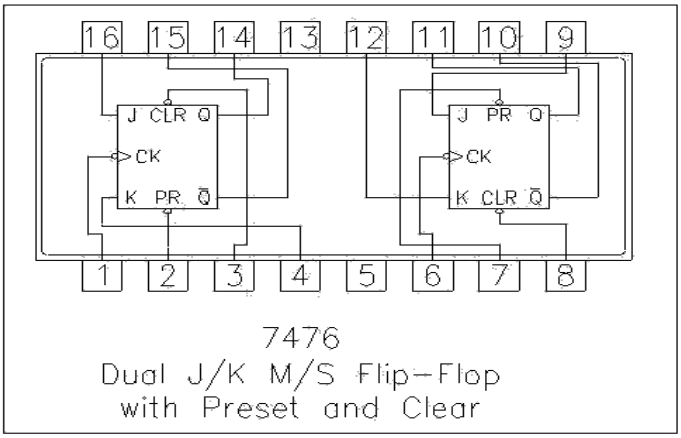
Aim: Design and verify the 4-bit asynchronous counter.

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

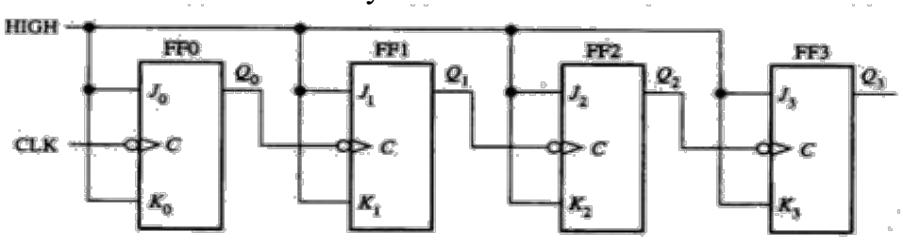
PIN CONFIGURATION:

Pin diagram of JK M/S Flip Flop



LOGIC DIAGRAM:

4-Bit Asynchronous counter



1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT:4-bit asynchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1How many flip-flops are required to make a MOD-32 binary counter?
Ans.5.
Q.2 The terminal count of a modulus-11 binary counter is _____.
Ans.1010.

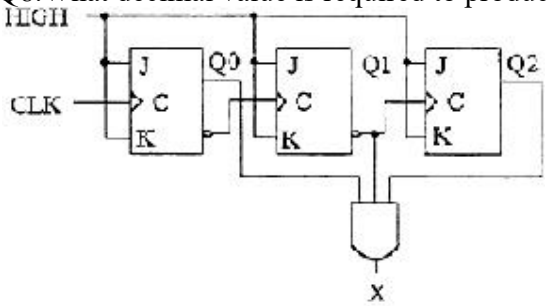
Q.3 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
Ans. Input clock pulses are applied simultaneously to each stage.
Q4.Synchronous construction reduces the delay time of a counter to the delay of:

Ans. a single flip-flop and a gate.

Q5.What is the difference between a 7490 and a 7492?

Ans.7490 is a MOD-10, 7492 is a MOD-12.

Q6.When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.
Ans. Product.
Q7. A BCD counter is a _____.
Ans. decade counter.
Q8.What decimal value is required to produce an output at "X" ?



Ans.5.

Q9.How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?
Ans. 64 gates, 6 inputs to each gate.
Q.10 A ring counter consisting of five Flip-Flops will have
Ans. 5 states.