

UNIT 5

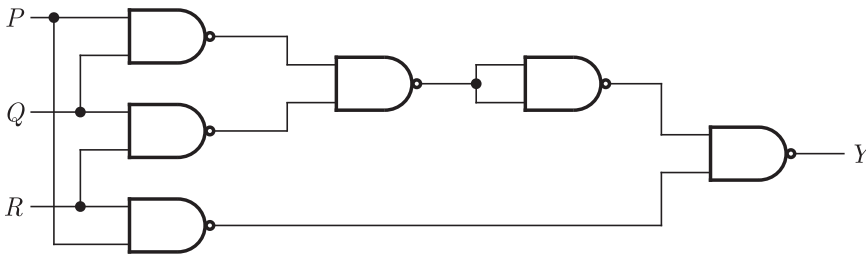
Digital Circuits

2011

ONE MARK

MCQ 5.1

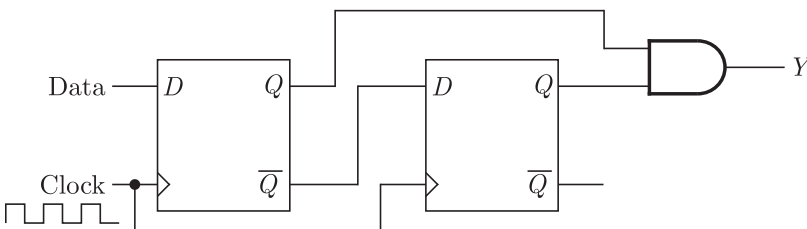
The output Y in the circuit below is always '1' when



- (A) two or more of the inputs P, Q, R are '0'
- (B) two or more of the inputs P, Q, R are '1'
- (C) any odd number of the inputs P, Q, R is '0'
- (D) any odd number of the inputs P, Q, R is '1'

MCQ 5.2

When the output Y in the circuit below is "1", it implies that data has



- (A) changed from "0" to "1"
- (B) changed from "1" to "0"
- (C) changed in either direction
- (D) not changed

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia

Published by: **NODIA and COMPANY**

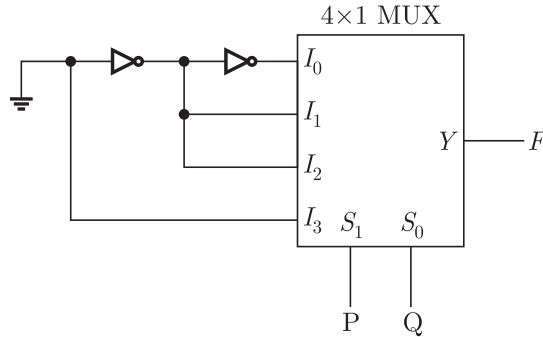
ISBN: **9788192276236**

Visit us at: www.nodia.co.in



MCQ 5.3

The logic function implemented by the circuit below is (ground implies a logic “0”)



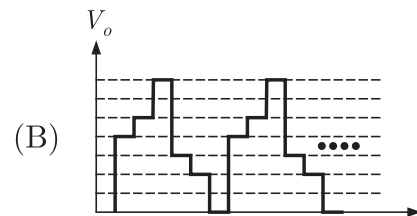
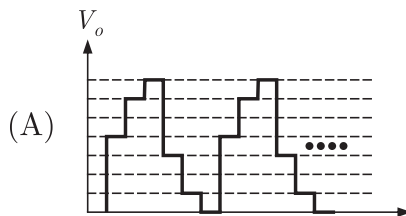
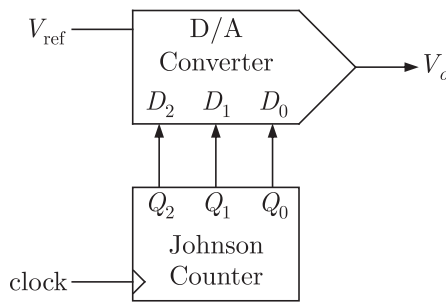
- (A) $F = \text{AND}(P, Q)$
- (B) $F = \text{OR}(P, Q)$
- (C) $F = \text{XNOR}(P, Q)$
- (D) $F = \text{XOR}(P, Q)$

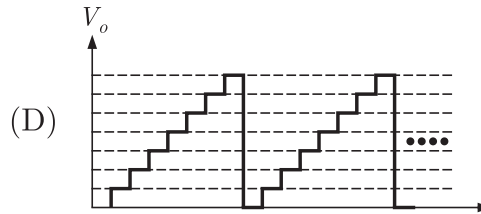
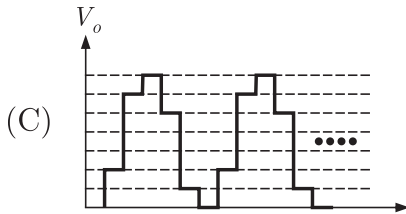
2011

TWO MARKS

MCQ 5.4

The output of a 3-stage Johnson (twisted ring) counter is fed to a digital-to analog (D/A) converter as shown in the figure below. Assume all states of the counter to be unset initially. The waveform which represents the D/A converter output V_o is





MCQ 5.5

Two D flip-flops are connected as a synchronous counter that goes through the following $Q_B Q_A$ sequence $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \dots$

The connections to the inputs D_A and D_B are

- (A) $D_A = Q_B, D_B = Q_A$
- (B) $D_A = \overline{Q_A}, D_B = \overline{Q_B}$
- (C) $D_A = (Q_A \overline{Q_B} + \overline{Q_A} Q_B), D_B = Q_A$
- (D) $D_A = (Q_A Q_B + \overline{Q_A} \overline{Q_B}), D_B = \overline{Q_B}$

MCQ 5.6

An 8085 assembly language program is given below. Assume that the carry flag is initially unset. The content of the accumulator after the execution of the program is

```

MVI  A, 07H
RLC
MOV  B, A
RLC
RLC
ADD  B
RRC
    
```

- (A) 8CH
- (B) 64H
- (C) 23H
- (D) 15H

2010 **ONE MARK**

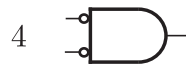
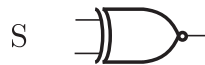
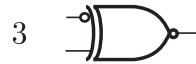
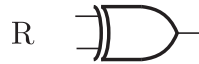
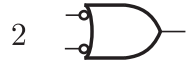
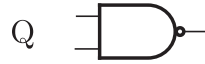
MCQ 5.7

Match the logic gates in **Column A** with their equivalents in **Column B**



Column A

Column B

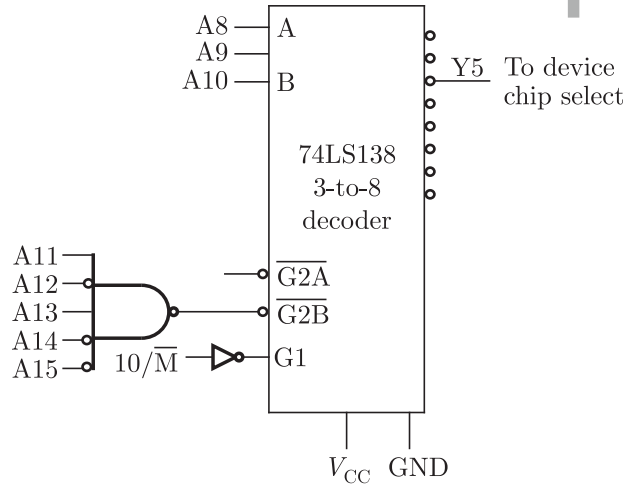


- (A) P-2, Q-4, R-1, S-3
(C) P-2, Q-4, R-3, S-1

- (B) P-4, Q-2, R-1, S-3
(D) P-4, Q-2, R-3, S-1

MCQ 5.8

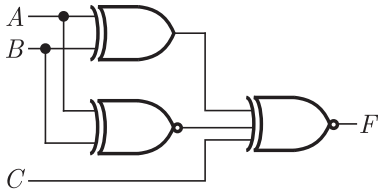
In the circuit shown, the device connected Y5 can have address in the range



- (A) 2000 - 20FF (B) 2D00 - 2DFF
(C) 2E00 - 2EFF (D) FD00 - FDFE

MCQ 5.9

For the output F to be 1 in the logic circuit shown, the input combination should be

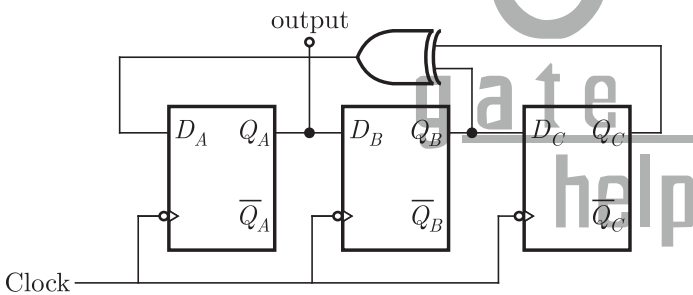


- (A) $A = 1, B = 1, C = 0$ (B) $A = 1, B = 0, C = 0$
 (C) $A = 0, B = 1, C = 0$ (D) $A = 0, B = 0, C = 1$

2010 **TWO MARKS**

MCQ 5.10

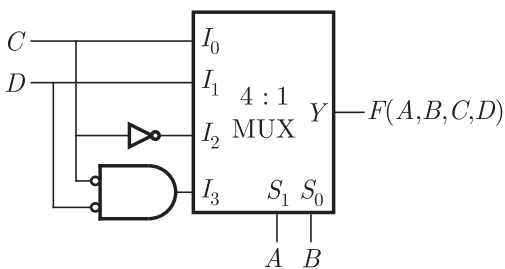
Assuming that the flip-flop are in reset condition initially, the count sequence observed at Q_A , in the circuit shown is



- (A) 0010111... (B) 0001011...
 (C) 0101111... (D) 0110100....

MCQ 5.11

The Boolean function realized by the logic circuit shown is



- (A) $F = \sum m(0, 1, 3, 5, 9, 10, 14)$ (B) $F = \sum m(2, 3, 5, 7, 8, 12, 13)$
 (C) $F = \sum m(1, 2, 4, 5, 11, 14, 15)$ (D) $F = \sum m(2, 3, 5, 7, 8, 9, 12)$



**MCQ 5.12**

For the 8085 assembly language program given below, the content of the accumulator after the execution of the program is

3000	MVI	A,	45H
3002	MOV	B,	A
3003	STC		
3004	CMC		
3005	RAR		
3006	XRA	B	

- (A) 00H (B) 45H
(C) 67H (D) E7H

2009**ONE MARK****MCQ 5.13**

The full form of the abbreviations TTL and CMOS in reference to logic families are

- (A) Triple Transistor Logic and Chip Metal Oxide Semiconductor
(B) Tristate Transistor Logic and Chip Metal Oxide Semiconductor
(C) Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
(D) Tristate Transistor Logic and Complementary Metal Oxide Silicon

MCQ 5.14

In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is

- (A) non-maskable and non-vectored
(B) maskable and non-vectored
(C) non-maskable and vectored
(D) maskable and vectored

2009

TWO MARKS

MCQ 5.15

If $X = 1$ in logic equation $[X + Z\{\bar{Y} + (\bar{Z} + XY)\}]\{\bar{X} + \bar{X}(X + Y)\} = 1$, then

- (A) $Y = Z$ (B) $Y = \bar{Z}$
(C) $Z = 1$ (D) $Z = 0$

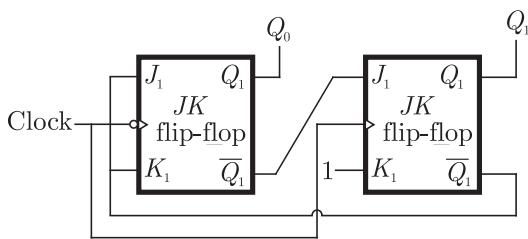
MCQ 5.16

What are the minimum number of 2- to -1 multiplexers required to generate a 2- input AND gate and a 2- input Ex-OR gate

- (A) 1 and 2 (B) 1 and 3
(C) 1 and 1 (D) 2 and 2

MCQ 5.17

What are the counting states (Q_1, Q_2) for the counter shown in the figure below



- (A) 11, 10, 00, 11, 10, ... (B) 01, 10, 11, 00, 01, ...
(C) 00, 11, 01, 10, 00, ... (D) 01, 10, 00, 01, 10, ...

Statement for Linked Answer Question 5.18 & 5.19 :

Two products are sold from a vending machine, which has two push buttons P_1 and P_2 .

When a button is pressed, the price of the corresponding product is displayed in a 7 - segment display. If no buttons are pressed, '0' is displayed signifying 'Rs 0'.

If only P_1 is pressed, '2' is displayed, signifying 'Rs. 2'

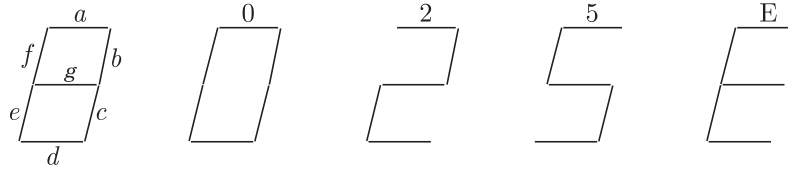
If only P_2 is pressed '5' is displayed, signifying 'Rs. 5'





If both P_1 and P_2 are pressed, 'E' is displayed, signifying 'Error'

The names of the segments in the 7 - segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.



Consider

- (1) push buttons pressed/not pressed in equivalent to logic 1/0 respectively.
- (2) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively.

MCQ 5.18

If segments a to g are considered as functions of P_1 and P_2 , then which of the following is correct

- (A) $g = \overline{P_1} + P_2$, $d = c + e$ (B) $g = P_1 + P_2$, $d = c + e$
 (C) $g = \overline{P_1} + P_2$, $e = b + c$ (D) $g = P_1 + P_2$, $e = b + c$

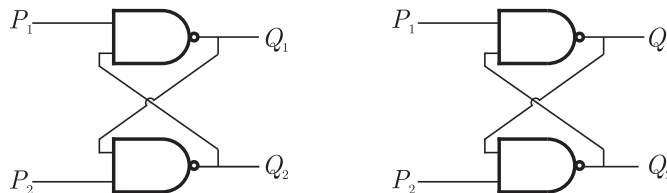
MCQ 5.19

What are the minimum numbers of NOT gates and 2 - input OR gates required to design the logic of the driver for this 7 - Segment display

- (A) 3 NOT and 4 OR (B) 2 NOT and 4 OR
 (C) 1 NOT and 3 OR (D) 2 NOT and 3 OR

MCQ 5.20

Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both latches are first made $(0, 1)$ and then, after a few seconds, made $(1, 1)$. The corresponding stable outputs (Q_1, Q_2) are



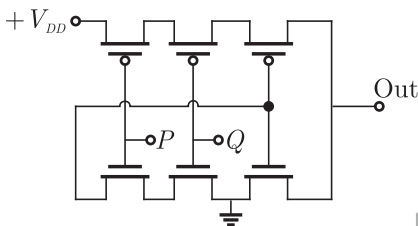
- (A) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
 (B) NAND : first (1, 0) then (1, 0) NOR : first (1, 0) then (1, 0)
 (C) NAND : first (1, 0) then (1, 0) NOR : first (1, 0) then (0, 0)
 (D) NAND : first (1, 0) then (1, 1) NOR : first (0, 1) then (0, 1)

2008

TWO MARKS

MCQ 5.21

The logic function implemented by the following circuit at the terminal OUT is



- (A) $P \text{ NOR } Q$ (B) $P \text{ NAND } Q$
 (C) $P \text{ OR } Q$ (D) $P \text{ AND } Q$

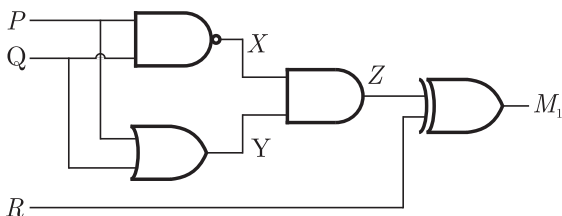
MCQ 5.22

The two numbers represented in signed 2's complement form are $P + 11101101$ and $Q = 11100110$. If Q is subtracted from P , the value obtained in signed 2's complement is

- (A) 1000001111 (B) 00000111
 (C) 11111001 (D) 11111001

MCQ 5.23

Which of the following Boolean Expressions correctly represents the relation between P, Q, R and M_1

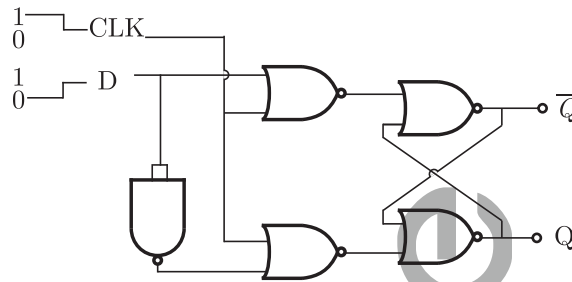




- (A) $M_1 = (P \text{ OR } Q) \text{ XOR } R$ (B) $M_1 = (P \text{ AND } Q) \text{ XOR } R$
 (C) $M_1 = (P \text{ NOR } Q) \text{ XOR } R$ (D) $M_1 = (P \text{ XOR } Q) \text{ XOR } R$

MCQ 5.24

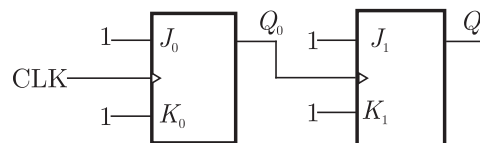
For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible. Which of the following statements is true?



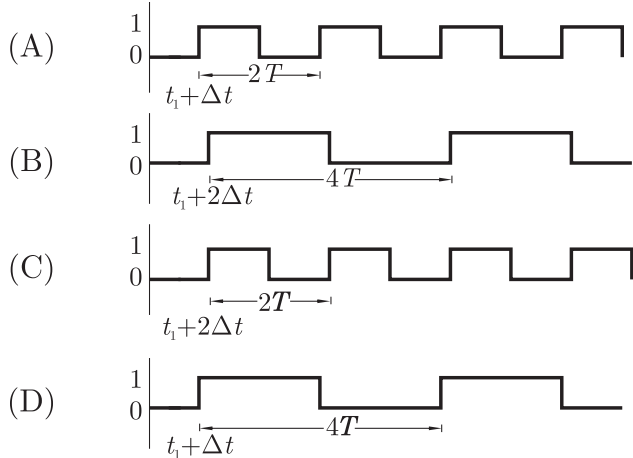
- (A) Q goes to 1 at the CLK transition and stays at 1
 (B) Q goes to 0 at the CLK transition and stays 0
 (C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1
 (D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

MCQ 5.25

For each of the positive edge-triggered $J-K$ flip flop used in the following figure, the propagation delay is Δt .

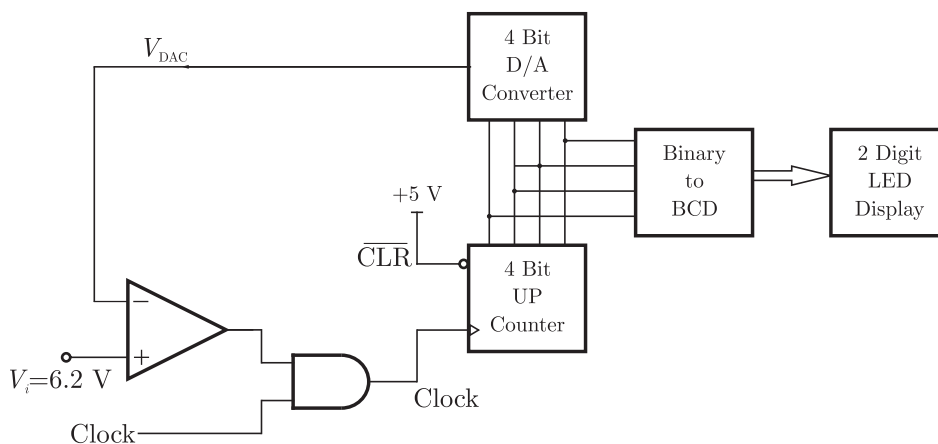


Which of the following wave forms correctly represents the output at Q_1 ?



Statement For Linked Answer Question 5.26 & 5.27 :

In the following circuit, the comparators output is logic "1" if $V_1 > V_2$ and is logic "0" otherwise. The D/A conversion is done as per the relation $V_{DAC} = \sum_{n=0}^3 2^{n-1} b_n$ Volts, where b_3 (MSB), b_1, b_2 and b_0 (LSB) are the counter outputs. The counter starts from the clear state.



MCQ 5.26

The stable reading of the LED displays is

- (A) 06
- (B) 07
- (C) 12
- (D) 13

**MCQ 5.27**

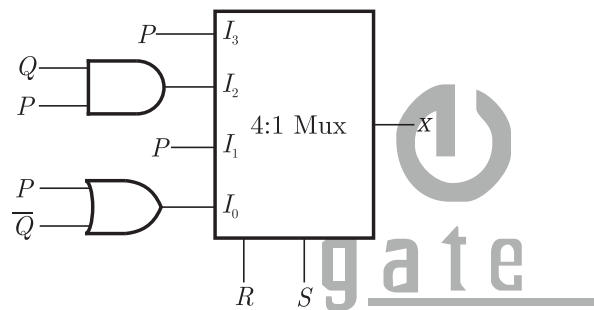
The magnitude of the error between V_{DAC} and V_{in} at steady state in volts is

- (A) 0.2 (B) 0.3
(C) 0.5 (D) 1.0

MCQ 5.28

For the circuit shown in the following, $I_0 - I_3$ are inputs to the 4:1 multiplexers, R (MSB) and S are control bits.

The output Z can be represented by



- (A) $PQ + P\bar{Q}S + \bar{Q}RS$
(B) $P\bar{Q} + PQR + \bar{P}QS$
(C) $P\bar{Q}R + \bar{P}QR + PARS + \bar{Q}RS$
(D) $P\bar{Q}R + PQR\bar{S} + P\bar{Q}RS + \bar{Q}RS$

MCQ 5.29

An 8085 executes the following instructions

2710 LXI H, 30A0 H

2713 DAD H

2414 PCHL

All address and constants are in Hex. Let PC be the contents of the program counter and HL be the contents of the HL register pair just after executing PCHL. Which of the following statements is correct ?

- (A) PC = 2715H (B) PC = 30A0H
HL = 30A0H HL = 2715H
(C) PC = 6140H (D) PC = 6140H
HL = 6140H HL = 2715H

2007

ONE MARK

MCQ 5.30

$X = 01110$ and $Y = 11001$ are two 5-bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is

- (A) 100111 (B) 0010000
(C) 000111 (D) 101001

MCQ 5.31

The Boolean function $Y = AB + CD$ is to be realized using only 2 - input NAND gates. The minimum number of gates required is

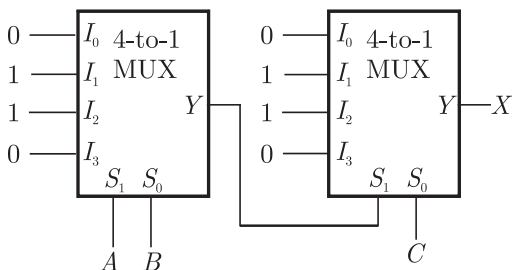
- (A) 2 (B) 3
(C) 4 (D) 5

2007

TWO MARKS

MCQ 5.32

In the following circuit, X is given by



- (A) $X = \overline{ABC} + \overline{A}BC + \overline{A}B\overline{C} + \overline{A}BC$
(B) $X = \overline{A}BC + \overline{A}B\overline{C} + \overline{A}BC + \overline{A}BC$
(C) $X = AB + BC + AC$
(D) $X = \overline{AB} + \overline{BC} + \overline{AC}$

MCQ 5.33

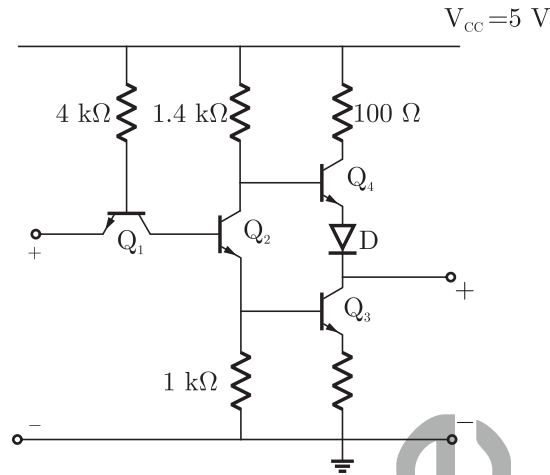
The Boolean expression $Y = \overline{ABC}D + \overline{A}BCD + \overline{A}BC\overline{D} + \overline{A}BC\overline{D}$ can be minimized to

- (A) $Y = \overline{ABC}D + \overline{A}BC + \overline{A}C\overline{D}$ (B) $Y = \overline{ABC}D + \overline{BC}D + \overline{A}BC\overline{D}$
(C) $Y = \overline{ABC}D + \overline{BC}D + \overline{A}BC\overline{D}$ (D) $Y = \overline{ABC}D + \overline{BC}D + \overline{A}BC\overline{D}$



**MCQ 5.34**

The circuit diagram of a standard *TTL* NOT gate is shown in the figure. $V_i = 25 \text{ V}$, the modes of operation of the transistors will be



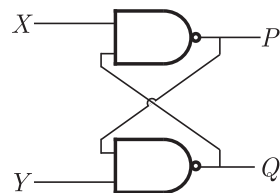
- (A) Q_1 : reverse active; Q_2 : normal active; Q_3 : saturation; Q_4 : cut-off
 (B) Q_1 : reverse active; Q_2 : saturation; Q_3 : saturation; Q_4 : cut-off
 (C) Q_1 : normal active; Q_2 : cut-off; Q_3 : cut-off; Q_4 : saturation
 (D) Q_1 : saturation; Q_2 : saturation; Q_3 : saturation; Q_4 : normal active

MCQ 5.35

The following binary values were applied to the X and Y inputs of NAND latch shown in the figure in the sequence indicated below :

$$X = 0, Y = 1; X = 0, Y = 0; X = 1; Y = 1$$

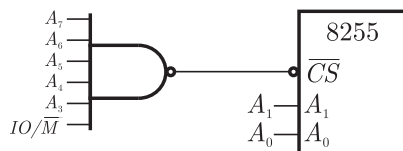
The corresponding stable P, Q output will be.



- (A) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$
 (B) $P = 1, Q = 0; P = 0, Q = 1; \text{ or } P = 0, Q = 1; P = 0, Q = 1$
 (C) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$ or $P = 0, Q = 1$
 (D) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$

MCQ 5.36

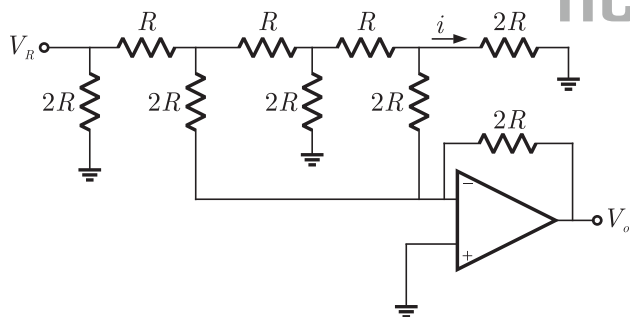
An 8255 chip is interfaced to an 8085 microprocessor system as an I/O mapped I/O as show in the figure. The address lines A_0 and A_1 of the 8085 are used by the 8255 chip to decode internally its three ports and the Control register. The address lines A_3 to A_7 as well as the IO/\overline{M} signal are used for address decoding. The range of addresses for which the 8255 chip would get selected is



- (A) F8H - FBH
(B) F8GH - FCH
(C) F8H - FFH
(D) F0H - F7H

Statement for Linked Answer Question 5.37 and 5.38 :

In the Digital-to-Analog converter circuit shown in the figure below, $V_R = 10\text{ V}$ and $R = 10\text{ k}\Omega$

**MCQ 5.37**

The current is

- (A) $31.25\mu\text{ A}$
(B) $62.5\mu\text{ A}$
(C) $125\mu\text{ A}$
(D) $250\mu\text{ A}$

MCQ 5.38

The voltage V_0 is

- (A) -0.781 V
(B) -1.562 V
(C) -3.125 V
(D) -6.250 V





Statement for Linked Answer Questions 5.39 & 5.40 :

An 8085 assembly language program is given below.

```

Line 1:      MVI A, B5H
           2:      MVI B, OEH
           3:      XRI 69H
           4:      ADD B
           5:      ANI 9BH
           6:      CPI 9FH
           7:      STA 3010H
           8:      HLT
  
```

MCQ 5.39

The contents of the accumulator just execution of the ADD instruction in line 4 will be

- (A) C3H (B) EAH
 (C) DCH (D) 69H

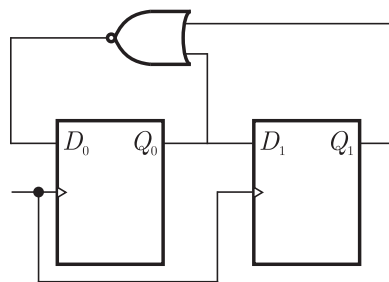
MCQ 5.40

After execution of line 7 of the program, the status of the *CY* and *Z* flags will be

- (A) $CY = 0, Z = 0$ (B) $CY = 0, Z = 1$
 (C) $CY = 1, Z = 0$ (D) $CY = 1, Z = 1$

MCQ 5.41

For the circuit shown, the counter state ($Q_1 Q_0$) follows the sequence



- (A) 00,01,10,11,00 (B) 00,01,10,00,01
 (C) 00,01,11,00,01 (D) 00,10,11,00,10

2006

ONE MARK

MCQ 5.42

The number of product terms in the minimized sum-of-product expression obtained through the following K - map is (where, "d" denotes don't care states)

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

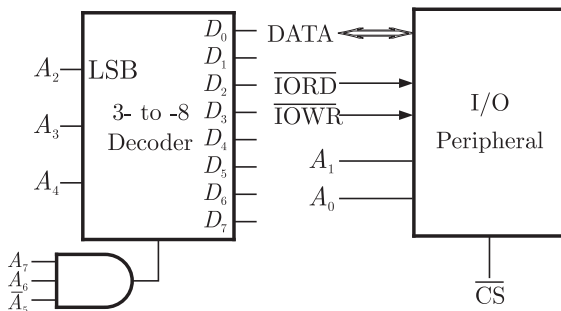
- (A) 2 (B) 3
(C) 4 (D) 5

2006

TWO MARKS

MCQ 5.43

An I/O peripheral device shown in Fig. (b) below is to be interfaced to an 8085 microprocessor. To select the I/O device in the I/O address range D4 H - D7 H, its chip-select (\overline{CS}) should be connected to the output of the decoder shown in as below :



- (A) output 7 (B) output 5
(C) output 2 (D) output 0

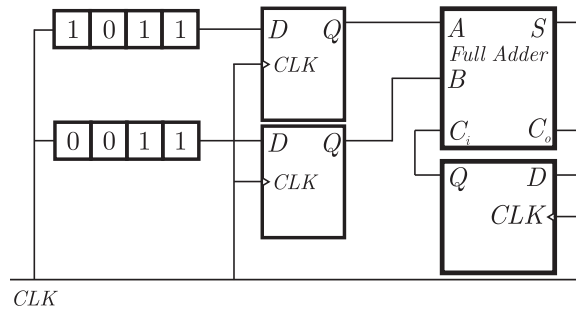
MCQ 5.44

For the circuit shown in figures below, two 4 - bit parallel - in serial - out shift registers loaded with the data shown are used to feed the





data to a full adder. Initially, all the flip - flops are in clear state. After applying two clock pulse, the output of the full-adder should be



- (A) $S = 0, C_0 = 0$
- (B) $S = 0, C_0 = 1$
- (C) $S = 1, C_0 = 0$
- (D) $S = 1, C_0 = 1$

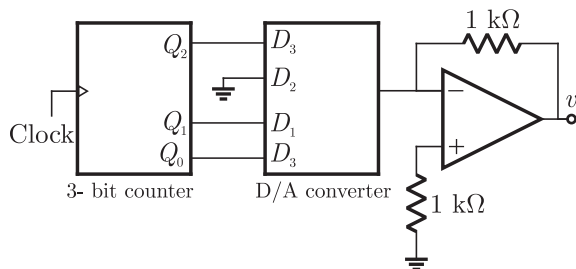
MCQ 5.45

A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this numbering system, the BCP code 10001001101 corresponds of the following number is base-5 system

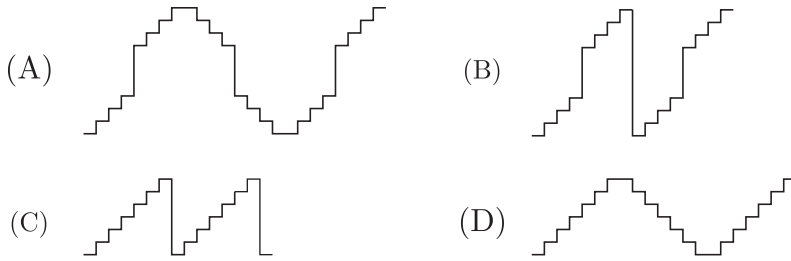
- (A) 423
- (B) 1324
- (C) 2201
- (D) 4231

MCQ 5.46

A 4 - bit D/A converter is connected to a free - running 3 - bit UP counter, as shown in the following figure. Which of the following waveforms will be observed at V_0 ?



In the figure shown above, the ground has been shown by the symbol ∇



MCQ 5.47

Following is the segment of a 8085 assembly language program

```
LXI SP, EFFF H
CALL 3000 H
:
:
:
3000 H LXI H, 3CF4
PUSH PSW
SPHL
POP PSW
RET
```



On completion of RET execution, the contents of SP is

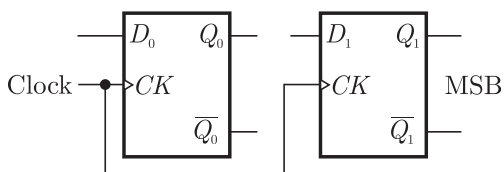
- (A) 3CF0 H
- (B) 3CF8 H
- (C) EFFF H
- (D) EFFF H

MCQ 5.48

Two *D* - flip - flops, as shown below, are to be connected as a synchronous counter that goes through the following sequence

00 → 01 → 11 → 10 → 00 → ...

The inputs *D*₀ and *D*₁ respectively should be connected as,

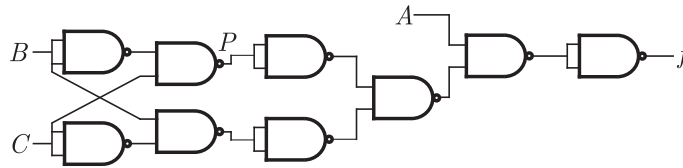




- (A) $\overline{Q_1}$ and Q_0 (B) $\overline{Q_0}$ and Q_1
 (C) $\overline{Q_1} Q_0$ and $\overline{Q_1} Q_0$ (D) $\overline{Q_1} \overline{Q_0}$ and $Q_1 Q_0$

MCQ 5.49

The point P in the following figure is stuck at 1. The output f will be



- (A) $ABC\overline{C}$ (B) \overline{A}
 (C) $ABC\overline{C}$ (D) A

2005

ONE MARK

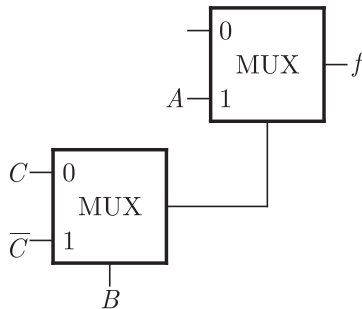
MCQ 5.50

Decimal 43 in Hexadecimal and BCD number system is respectively

- (A) B2, 0100 011 (B) 2B, 0100 0011
 (C) 2B, 0011 0100 (D) B2, 0100 0100

MCQ 5.51

The Boolean function f implemented in the figure using two input multiplexes is



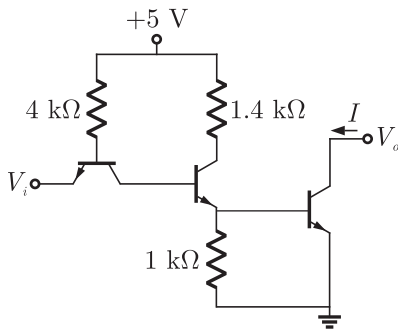
- (A) $A\overline{B}C + ABC\overline{C}$ (B) $ABC + \overline{ABC}$
 (C) $\overline{ABC} + \overline{ABC}$ (D) $\overline{ABC} + \overline{ABC}$

2005

TWO MARKS

MCQ 5.52

The transistors used in a portion of the TTL gate show in the figure have $\beta = 100$. The base emitter voltage of is 0.7 V for a transistor in active region and 0.75 V for a transistor in saturation. If the sink current $I = 1$ A and the output is at logic 0, then the current I_R will be equal to



- (A) 0.65 mA
(C) 0.75 mA

- (B) 0.70 mA
(D) 1.00 mA

MCQ 5.53

The Boolean expression for the truth table shown is

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- (A) $B(A + C)(\bar{A} + \bar{C})$
(C) $\bar{B}(A + \bar{C})(\bar{A} + C)$

- (B) $B(A + \bar{C})(\bar{A} + C)$
(D) $\bar{B}(A + C)(\bar{A} + \bar{C})$

MCQ 5.54

The present output Q_n of an edge triggered JK flip-flop is logic 0. If $J = 1$, then Q_{n+1}

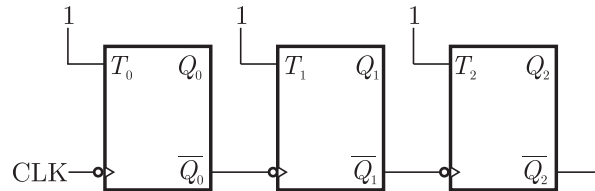




- (A) Cannot be determined
- (B) Will be logic 0
- (C) will be logic 1
- (D) will rave around

MCQ 5.55

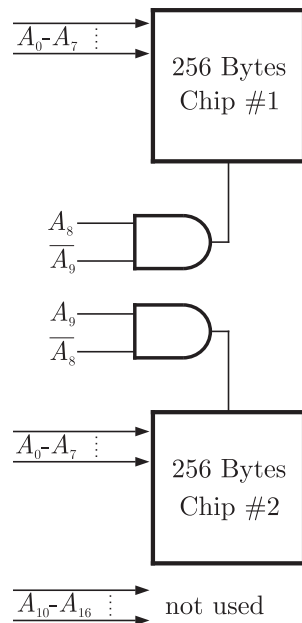
The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2 Q_1 Q_0 = 001$ then is next state $Q_2 Q_1 Q_0$ will be



- (A) 010
- (B) 111
- (C) 100
- (D) 101

MCQ 5.56

What memory address range is NOT represents by chip # 1 and chip # 2 in the figure A_0 to A_{15} in this figure are the address lines and CS means chip select.



- (A) 0100 - 02FF
- (B) 1500 - 16FF
- (C) F900 - FAFF
- (D) F800 - F9FF

Statement For Linked Answer Questions 5.57 & 5.58 :

Consider an 8085 microprocessor system.

MCQ 5.57

The following program starts at location 0100H.

```
LXI SP, 00FF
```

```
LXI H, 0701
```

```
MVI A, 20H
```

```
SUB M
```

The content of accumulator when the program counter reaches 0109 H is

(A) 20 H

(B) 02 H

(C) 00 H

(D) FF H

MCQ 5.58

If in addition following code exists from 019H onwards,

```
ORI 40 H
```

```
ADD M
```

What will be the result in the accumulator after the last instruction is executed ?

(A) 40 H

(B) 20 H

(C) 60 H

(D) 42 H

2004**ONE MARK****MCQ 5.59**

A master - slave flip flop has the characteristic that

(A) change in the output immediately reflected in the output

(B) change in the output occurs when the state of the master is affected

(C) change in the output occurs when the state of the slave is affected

(D) both the master and the slave states are affected at the same time



gate
help

**MCQ 5.60**

The range of signed decimal numbers that can be represented by 6-bits 1's complement number is

- (A) -31 to +31 (B) -63 to +63
(C) -64 to +63 (D) -32 to +31

MCQ 5.61

A digital system is required to amplify a binary-encoded audio signal. The user should be able to control the gain of the amplifier from minimum to a maximum in 100 increments. The minimum number of bits required to encode, in straight binary, is

- (A) 8 (B) 6
(C) 5 (D) 7

MCQ 5.62

Choose the correct one from among the alternatives A, B, C, D after matching an item from Group 1 most appropriate item in Group 2.

Group 1

P. Shift register

Q. Counter

R. Decoder

(A) $P - 3, Q - 2, R - 1$

(C) $P - 2, Q - 1, R - 3$

Group 2

1. Frequency division

2. Addressing in memory chips

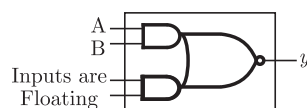
3. Serial to parallel data conversion

(B) $P - 3, Q - 1, R - 2$

(D) $P - 1, Q - 2, R - 2$

MCQ 5.63

The figure the internal schematic of a TTL AND-OR-OR-Invert (AOI) gate. For the inputs shown in the figure, the output Y is



- (A) 0 (B) 1
(C) AB (D) \overline{AB}

2004

TWO MARKS

MCQ 5.64

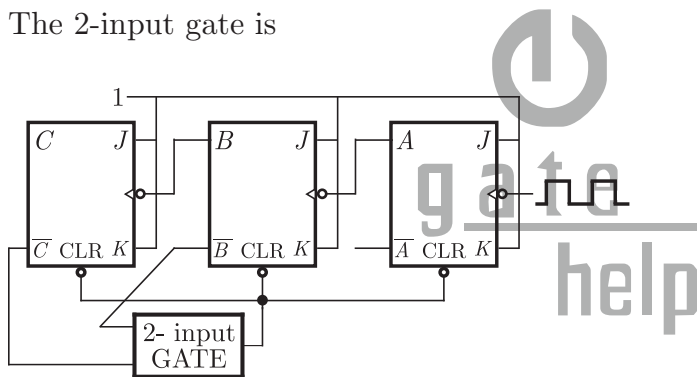
11001, 1001, 111001 correspond to the 2's complement representation of which one of the following sets of number

- (A) 25, 9, and 57 respectively (B) -6, -6, and -6 respectively
(C) -7, -7 and -7 respectively (D) -25, -9 and -57 respectively

MCQ 5.65

In the modulo-6 ripple counter shown in figure, the output of the 2-input gate is used to clear the J-K flip-flop

The 2-input gate is



- (A) a NAND gate (B) a NOR gate
(C) an OR gate (D) a AND gate

MCQ 5.66

The minimum number of 2- to -1 multiplexers required to realize a 4- to -1 multiplexers is

- (A) 1 (B) 2
(C) 3 (D) 4

MCQ 5.67

The Boolean expression $AC + B\bar{C}$ is equivalent to

- (A) $\bar{A}C + B\bar{C} + AC$ (B) $\bar{B}C + AC + B\bar{C} + \bar{A}C\bar{B}$
(C) $AC + B\bar{C} + \bar{B}C + ABC$ (D) $ABC + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}C$



**MCQ 5.68**

A Boolean function f of two variables x and y is defined as follows :

$$f(0,0) = f(0,1) = f(1,1) = 1; f(1,0) = 0$$

Assuming complements of x and y are not available, a minimum cost solution for realizing f using only 2-input NOR gates and 2- input OR gates (each having unit cost) would have a total cost of

- (A) 1 unit (B) 4 unit
(C) 3 unit (D) 2 unit

MCQ 5.69

The 8255 Programmable Peripheral Interface is used as described below.

(i) An A/D converter is interface to a microprocessor through an 8255.

The conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be stobed into Port A.

(ii) Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals.

The appropriate modes of operation of the 8255 for (i) and (ii) would be

- (A) Mode 0 for (i) and Mode 1 for (ii)
(B) Mode 1 for (i) and Mode 2 for (ii)
(C) Mode for (i) and Mode 0 for (ii)
(D) Mode 2 for (i) and Mode 1 for (ii)

MCQ 5.70

The number of memory cycles required to execute the following 8085 instructions

- (i) LDA 3000 H
(ii) LXI D, FOF1H

would be

- (A) 2 for (i) and 2 for (ii) (B) 4 for (i) and 3 for (ii)
(C) 3 for (i) and 3 for (ii) (D) 3 for (i) and 4 for (ii)

MCQ 5.71

Consider the sequence of 8085 instructions given below

LXI H, 9258

MOV A, M

CMA

MOV M, A

Which one of the following is performed by this sequence ?

- (A) Contents of location 9258 are moved to the accumulator
- (B) Contents of location 9258 are compared with the contents of the accumulator
- (C) Contents of location 8529 are complemented and stored in location 8529
- (D) Contents of location 5892 are complemented and stored in location 5892

MCQ 5.72

It is desired to multiply the numbers 0AH by 0BH and store the result in the accumulator. The numbers are available in registers B and C respectively. A part of the 8085 program for this purpose is given below :

MVI A, 00H

LOOP -----

HLT

END

The sequence of instructions to complete the program would be

- (A) JNX LOOP, ADD B, DCR C
- (B) ADD B, JNZ LOOP, DCR C
- (C) DCR C, JNZ LOOP, ADD B
- (D) ADD B, DCR C, JNZ LOOP



gate
help



2003

ONE MARK

MCQ 5.73

The number of distinct Boolean expressions of 4 variables is

- (A) 16 (B) 256
(C) 1023 (D) 65536

MCQ 5.74

The minimum number of comparators required to build an 8-bits flash ADC is

- (A) 8 (B) 63
(C) 255 (D) 256

MCQ 5.75

The output of the 74 series of GATE of TTL gates is taken from a BJT in

- (A) totem pole and common collector configuration
(B) either totem pole or open collector configuration
(C) common base configuration
(D) common collector configuration

MCQ 5.76

Without any additional circuitry, an 8:1 MUX can be used to obtain

- (A) some but not all Boolean functions of 3 variables
(B) all functions of 3 variables but non of 4 variables
(C) all functions of 3 variables and some but not all of 4 variables
(D) all functions of 4 variables

MCQ 5.77

A 0 to 6 counter consists of 3 flip flops and a combination circuit of 2 input gate (s). The common circuit consists of

- (A) one AND gate
(B) one OR gate
(C) one AND gate and one OR gate
(D) two AND gates

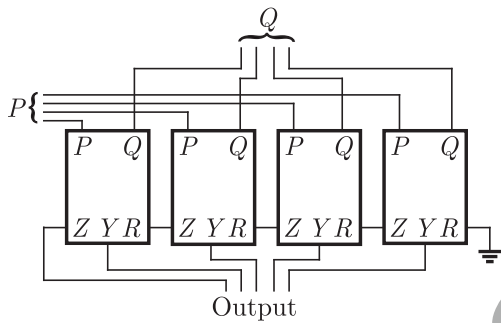
2003

TWO MARKS

MCQ 5.78

The circuit in the figure has 4 boxes each described by inputs P, Q, R and outputs Y, Z with $Y = P \oplus Q \oplus R$ and $Z = RQ + \overline{P}R + Q\overline{P}$

The circuit acts as a



- (A) 4 bit adder giving $P + Q$
 (B) 4 bit subtractor giving $P - Q$
 (C) 4 bit subtractor giving $Q - P$
 (D) 4 bit adder giving $P + Q + R$

MCQ 5.79

If the function W, X, Y and Z are as follows

$$W = R + \overline{P}Q + \overline{R}S \quad X = PQR\overline{S} + \overline{P}QR\overline{S} + P\overline{Q}R\overline{S}$$

$$Y = RS + \overline{P}R + \overline{P}Q + \overline{P}.\overline{Q} \quad Z = R + S + \overline{P}Q + \overline{P}.\overline{Q}.R + \overline{P}Q.\overline{S}$$

Then,

- (A) $W = Z, X = \overline{Z}$ (B) $W = Z, X = Y$
 (C) $W = Y$ (D) $W = Y = \overline{Z}$

MCQ 5.80

A 4 bit ripple counter and a bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

- (A) $R = 10$ ns, $S = 40$ ns (B) $R = 40$ ns, $S = 10$ ns
 (C) $R = 10$ ns, $S = 30$ ns (D) $R = 30$ ns, $S = 10$ ns



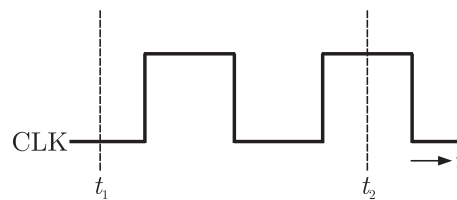
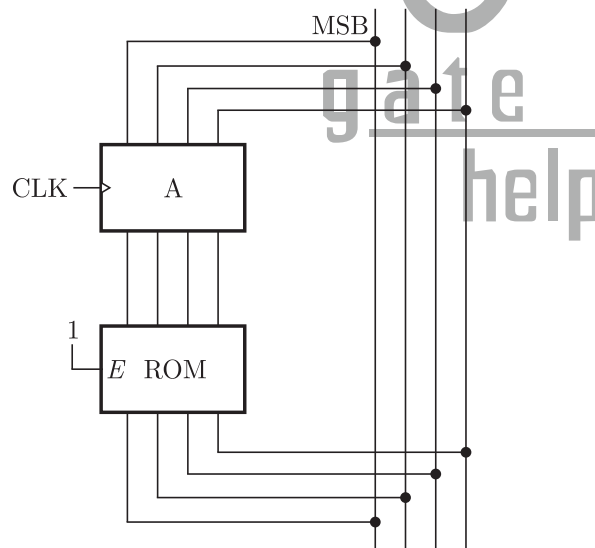


MCQ 5.81

In the circuit shown in the figure, A is parallel-in, parallel-out 4 bit register, which loads at the rising edge of the clock C . The input lines are connected to a 4 bit bus, W . Its output acts at input to a 16×4 ROM whose output is floating when the input to a partial table of the contents of the ROM is as follows

Data	0011	1111	0100	1010	1011	1000	0010	1000
Address	0	2	4	6	8	10	11	14

The clock to the register is shown, and the data on the W bus at time t_1 is 0110. The data on the bus at time t_2 is



- (A) 1111
- (B) 1011
- (C) 1000
- (D) 0010

MCQ 5.82

The DTL, TTL, ECL and CMOS famil GATE of digital ICs are compared in the following 4 columns

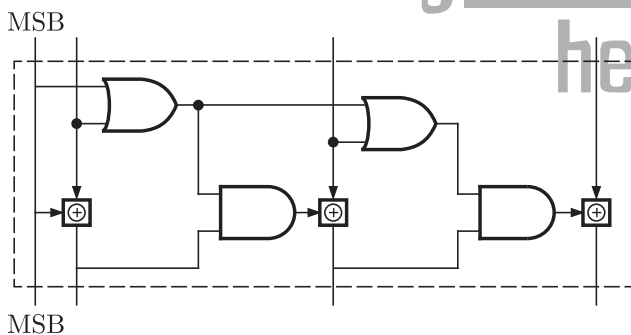
	(P)	(Q)	(R)	(S)
Fanout is minimum	DTL	DTL	TTL	CMOS
Power consumption is minimum	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

The correct column is

- (A) P (B) Q
(C) R (D) S

MCQ 5.83

The circuit shown in figure converts



- (A) BCD to binary code (B) Binary to excess - 3 code
(C) Excess -3 to gray code (D) Gray to Binary code

MCQ 5.84

In an 8085 microprocessor, the instruction CMP B has been executed while the content of the accumulator is less than that of register B . As a result

- (A) Carry flag will be set but Zero flag will be reset
(B) Carry flag will be rest but Zero flag will be set
(C) Both Carry flag and Zero flag will be rest
(D) Both Carry flag and Zero flag will be set



**MCQ 5.85**

The circuit shown in the figure is a 4 bit DAC

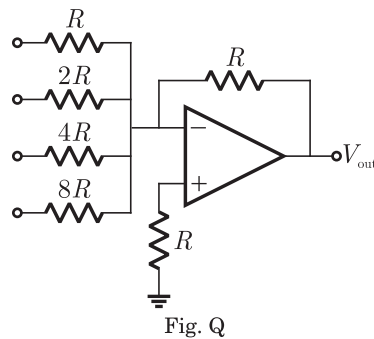


Fig. Q

The input bits 0 and 1 are represented by 0 and 5 V respectively. The OP AMP is ideal, but all the resistance and the 5 v inputs have a tolerance of $\pm 10\%$. The specification (rounded to nearest multiple of 5%) for the tolerance of the DAC is

- (A) $\pm 35\%$ (B) $\pm 20\%$
(C) $\pm 10\%$ (D) $\pm 5\%$

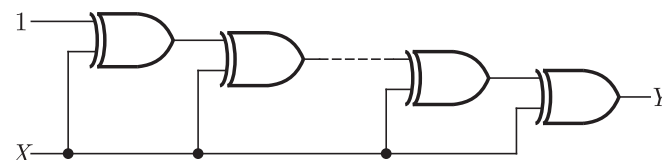
2002**ONE MARK****MCQ 5.86**

4 - bit 2's complement representation of a decimal number is 1000. The number is

- (A) +8 (B) 0
(C) -7 (D) -8

MCQ 5.87

If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR - gates is X , then the output Y is equal to



- (A) 0 (B) 1
(C) \bar{X} (D) X

MCQ 5.88

The number of comparators required in a 3-bit comparators type ADC

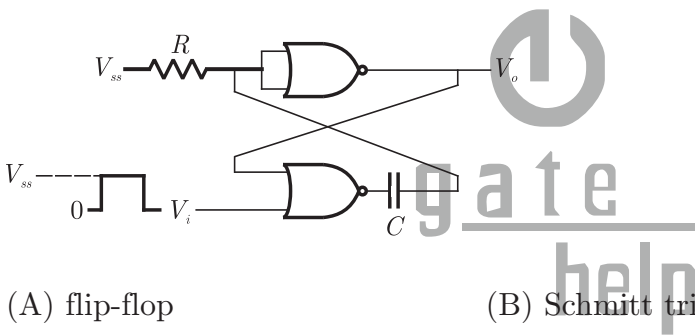
- (A) 2
- (B) 3
- (C) 7
- (D) 8

2002

TWO MARKS

MCQ 5.89

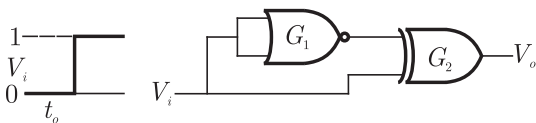
The circuit in the figure has two CMOS NOR gates. This circuit functions as a:



- (A) flip-flop
- (B) Schmitt trigger
- (C) Monostable multivibrator
- (D) astable multivibrator

MCQ 5.90

The gates G_1 and G_2 in the figure have propagation delays of 10 ns and 20 ns respectively. If the input V_1 , makes an output change from logic 0 to 1 at time $t = t_0$, then the output waveform V_0 is

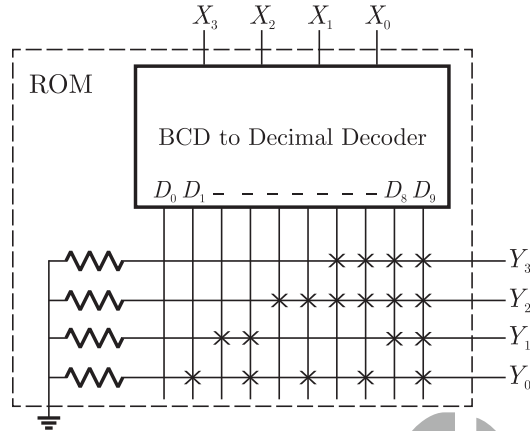


- (A)
- (B)
- (C)
- (D)



**MCQ 5.91**

If the input X_3, X_2, X_1, X_0 to the ROM in the figure are 8 4 2 1 BCD numbers, then the outputs Y_3, Y_2, Y_1, Y_0 are



- (A) gray code numbers (B) 2 4 2 1 BCD numbers
(C) excess - 3 code numbers (D) none of the above

MCQ 5.92

Consider the following assembly language program

```

MVI B, 87H
MOV A, B
START :   JMP NEXT
         MVI B, 00H
         XRA B
         OUT PORT1
         HLT
NEXT :   XRA B
         JP START
         OUT PORT2
         HTL

```

The execution of above program in an 8085 microprocessor will result in

- (A) an output of 87H at PORT1

- (B) an output of 87H at PORT2
- (C) infinite looping of the program execution with accumulator data remaining at 00H
- (D) infinite looping of the program execution with accumulator data alternating between 00H and 87H

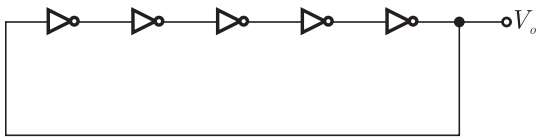
2001**ONE MARKS****MCQ 5.93**

The 2's complement representation of -17 is

- (A) 101110
- (B) 101111
- (C) 111110
- (D) 110001

MCQ 5.94

For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output



- (A) 10 MHz
- (B) 100 MHz
- (C) 1 GHz
- (D) 2 GHz

MCQ 5.95

An 8085 microprocessor based system uses a $4K \times 8$ bit RAM whose starting address is AA00H. The address of the last byte in this RAM is

- (A) OFFFH
- (B) 1000H
- (C) B9FFH
- (D) BA00H

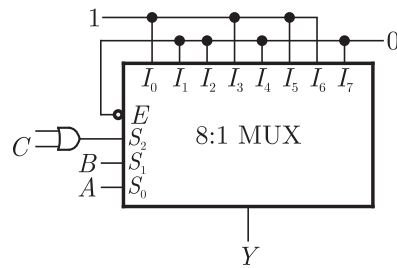
2001**TWO MARKS****MCQ 5.96**

In the TTL circuit in the figure, S_2 and S_0 are select lines and X_7 and





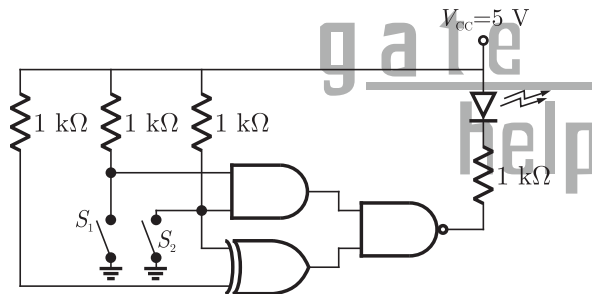
X_0 are input lines. S_0 and X_0 are LSBs. The output Y is



- (A) indeterminate
- (B) $A \oplus B$
- (C) $\overline{A \oplus B}$
- (D) $\overline{C}(\overline{A \oplus B}) + C(A \oplus B)$

MCQ 5.97

In the figure, the LED

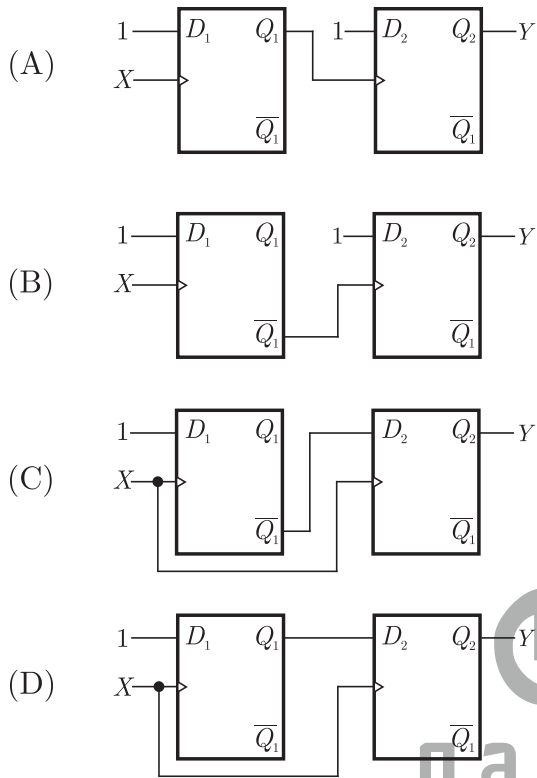


- (A) emits light when both S_1 and S_2 are closed
- (B) emits light when both S_1 and S_2 are open
- (C) emits light when only of S_1 and S_2 is closed
- (D) does not emit light, irrespective of the switch positions.

MCQ 5.98

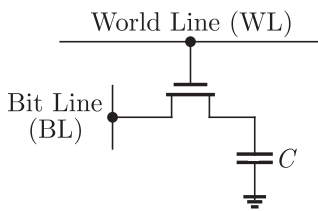
The digital block in the figure is realized using two positive edge triggered D-flip-flop. Assume that for $t < t_0$, $Q_1 = Q_2 = 0$. The circuit in the digital block is given by





MCQ 5.99

In the DRAM cell in the figure, the V_t of the NMOSFET is 1 V. For the following three combinations of WL and BL voltages.



- (A) 5 V; 3 V; 7 V (B) 4 V; 3 V; 4 V
(C) 5 V; 5 V; 5 V (D) 4 V; 4 V; 4 V

2000 **ONE MARKS**

MCQ 5.100

An 8 bit successive approximation analog to digital communication has full scale reading of 2.55 V and its conversion time for an analog



input of 1 V is $20 \mu s$. The conversion time for a 2 V input will be

- (A) $10 \mu s$ (B) $20 \mu s$
(C) $40 \mu s$ (D) $50 \mu s$

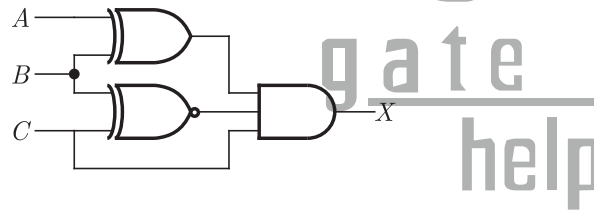
MCQ 5.101

The number of comparator in a 4-bit flash ADC is

- (A) 4 (B) 5
(C) 15 (D) 16

MCQ 5.102

For the logic circuit shown in the figure, the required input condition (A, B, C) to make the output (X) = 1 is



- (A) 1,0,1 (B) 0,0,1
(C) 1,1,1 (D) 0,1,1

MCQ 5.103

The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor are

- (A) 1 (B) 4
(C) 5 (D) 13

MCQ 5.104

In the microprocessor, the RST6 instruction transfer the program execution to the following location :

- (A) 30 H (B) 24 H
(C) 48 H (D) 60 H

2000

TWO MARKS

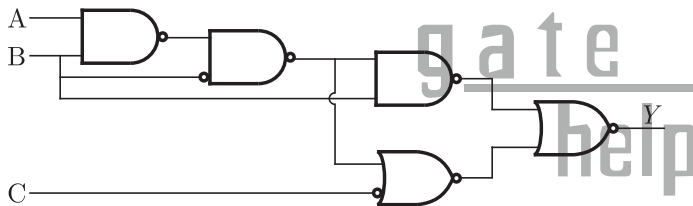
MCQ 5.105

The contents of register (B) and accumulator (A) of 8085 microprocessor are 49H and 3AH respectively. The contents of A and status of carry (CY) and sign (S) after execution SUB B instructions are

- (A) A = F1, CY = 1, S = 1
- (B) A = 0F, CY = 1, S = 1
- (C) A = F0, CY = 0, S = 0
- (D) A = 1F, CY = 1, S = 1

MCQ 5.106

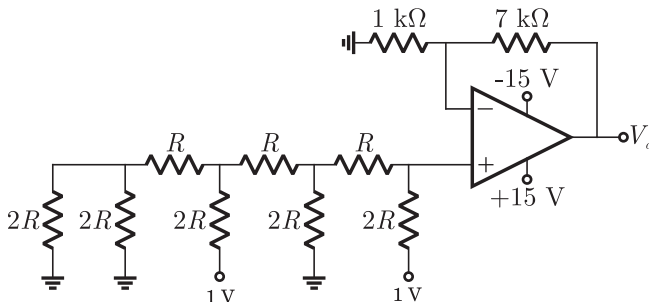
For the logic circuit shown in the figure, the simplified Boolean expression for the output Y is



- (A) $A + B + C$
- (B) A
- (C) B
- (D) C

MCQ 5.107

For the 4 bit DAC shown in the figure, the output voltage V_0 is



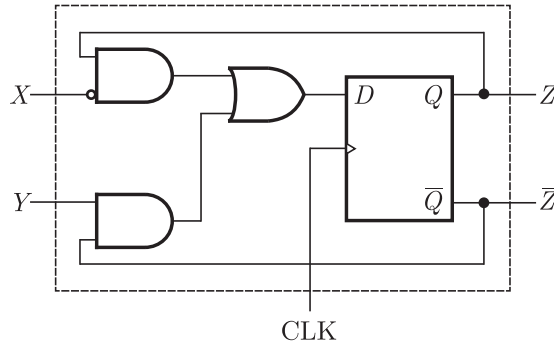
- (A) 10 V
- (B) 5 V
- (C) 4 V
- (D) 8 V





MCQ 5.108

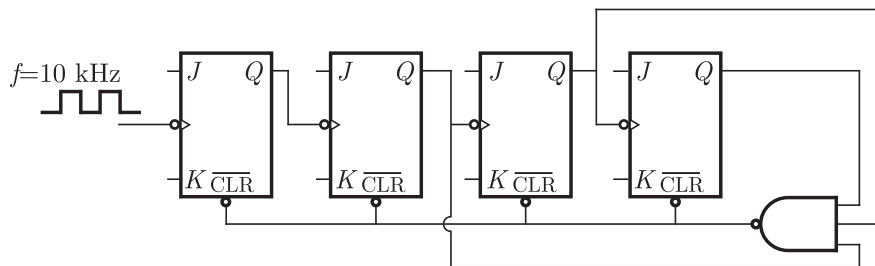
A sequential circuit using D flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the outputs. The circuit is



- (A) $S - R$ Flip-Flop with inputs $X = R$ and $Y = S$
- (B) $S - R$ Flip-Flop with inputs $X = S$ and $Y = R$
- (C) $J - K$ Flip-Flop with inputs $X = J$ and $Y = K$
- (D) $J - K$ Flip-Flop with inputs $X = K$ and $Y = J$

MCQ 5.109

In the figure, the J and K inputs of all the four Flip-Flops are made high. The frequency of the signal at output Y is



- (A) 0.833 kHz
- (B) 1.0 kHz
- (C) 0.91 kHz
- (D) 0.77 kHz

1999 **ONE MARK**

MCQ 5.110

The logical expression $y = A + \overline{A}B$ is equivalent to

- (A) $y = AB$ (B) $y = \overline{AB}$
 (C) $y = \overline{A} + B$ (D) $y = A + B$

MCQ 5.111

A Darlington emitter follower circuit is sometimes used in the output stage of a TTL gate in order to

- (A) increase its I_{OL}
 (B) reduce its I_{OH}
 (C) increase its speed of operation
 (D) reduce power dissipation

MCQ 5.112

Commercially available ECL gates use two ground lines and one negative supply in order to

- (A) reduce power dissipation
 (B) increase fan-out
 (C) reduce loading effect
 (D) eliminate the effect of power line glitches or the biasing circuit

MCQ 5.113

The resolution of a 4-bit counting ADC is 0.5 volts. For an analog input of 6.6 volts, the digital output of the ADC will be

- (A) 1011 (B) 1101
 (C) 1100 (D) 1110

1999**TWO MARKS****MCQ 5.114**

The minimized form of the logical expression

$(\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C})$ is

- (A) $\overline{A}\overline{C} + B\overline{C} + \overline{A}B$ (B) $A\overline{C} + \overline{B}C + \overline{A}B$
 (C) $\overline{A}C + \overline{B}C + \overline{A}B$ (D) $A\overline{C} + \overline{B}C + A\overline{B}$

MCQ 5.115

For a binary half-subtractor having two inputs A and B, the correct



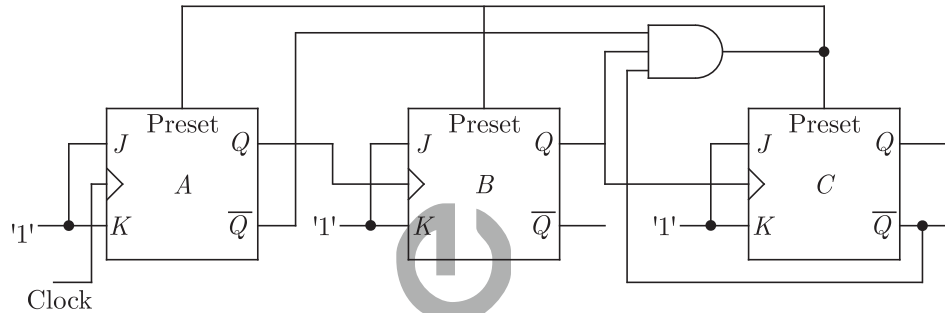


set of logical expressions for the outputs $D (= A \text{ minus } B)$ and $X (= \text{borrow})$ are

- (A) $D = AB + \bar{A}B, X = \bar{A}B$ (B) $D = \bar{A}B + A\bar{B} + A\bar{B}, X = A\bar{B}$
 (C) $D = \bar{A}B + A\bar{B}, X = \bar{A}B$ (D) $D = AB + \bar{A}\bar{B}, X = A\bar{B}$

MCQ 5.116

The ripple counter shown in the given figure is works as a



- (A) mod-3 up counter (B) mod-5 up counter
 (C) mod-3 down counter (D) mod-5 down counter

MCQ 5.117

If $CS = A_{15}A_{14}A_{13}$ is used as the chip select logic of a 4 K RAM in an 8085 system, then its memory range will be

- (A) 3000 H - 3 FFF H
 (B) 7000 H - 7 FFF H
 (C) 5000 H - 5 FFF H and 6000 H - 6 FFF H
 (D) 6000 H - 6 FFF H and 7000 H - 7 FFF H

1998

ONE MARK

MCQ 5.118

The minimum number of 2-input NAND gates required to implement of Boolean function $Z = A\bar{B}C$, assuming that A, B and C are available, is

- (A) two (B) three
 (C) five (D) six

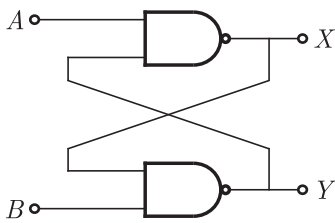
MCQ 5.119

The noise margin of a TTL gate is about

- (A) 0.2 V (B) 0.4 V
(C) 0.6 V (D) 0.8 V

MCQ 5.120

In the figure is $A = 1$ and $B = 1$, the input B is now replaced by a sequence 101010....., the output x and y will be



- (A) fixed at 0 and 1, respectively
(B) $x = 1010$while $y = 0101$
(C) $x = 1010$and $y = 1010$
(D) fixed at 1 and 0, respectively

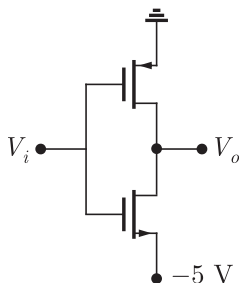
MCQ 5.121

An equivalent 2's complement representation of the 2's complement number 1101 is

- (A) 110100 (B) 01101
(C) 110111 (D) 111101

MCQ 5.122

The threshold voltage for each transistor in the figure is 2 V. For this circuit to work as an inverter, V_i must take the values





- (A) -5 V and 0 V (B) -5 V and 5 V
(C) -0 V and 3 V (D) 3 V and 5 V

MCQ 5.123

An I/O processor control the flow of information between

- (A) cache memory and I/O devices
(B) main memory and I/O devices
(C) two I/O devices
(D) cache and main memories

MCQ 5.124

Two 2's complement number having sign bits x and y are added and the sign bit of the result is z . Then, the occurrence of overflow is indicated by the Boolean function

- (A) xyz (B) $\bar{x}\bar{y}\bar{z}$
(C) $\bar{x}\bar{y}z + xy\bar{z}$ (D) $xy + yz + zx$

MCQ 5.125

The advantage of using a dual slope ADC in a digital voltmeter is that

- (A) its conversion time is small
(B) its accuracy is high
(C) it gives output in BCD format
(D) it does not require a

MCQ 5.126

For the identity $AB + \bar{A}C + BC = AB + \bar{A}C$, the dual form is

- (A) $(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$
(B) $(\bar{A} + \bar{B})(A + \bar{C})(\bar{B} + \bar{C}) = (\bar{A} + \bar{B})(A + \bar{C})$
(C) $(A + B)(\bar{A} + C)(B + C) = (\bar{A} + \bar{B})(A + \bar{C})$
(D) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C} = \bar{A}\bar{B} + A\bar{C}$

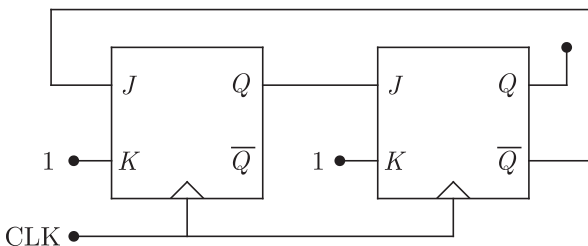
MCQ 5.127

An instruction used to set the carry Flag in a computer can be classified as

- (A) data transfer (B) arithmetic
(C) logical (D) program control

MCQ 5.128

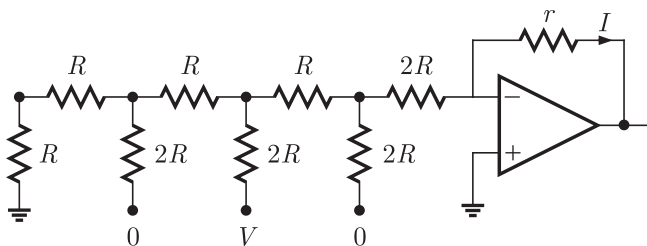
The figure is shows a mod-K counter, here K is equal to



- (A) 1 (B) 2
(C) 3 (D) 4

MCQ 5.129

The current I through resistance r in the circuit shown in the figure is



- (A) $\frac{-V}{12R}$ (B) $\frac{V}{12R}$
(C) $\frac{V}{6R}$ (D) $\frac{V}{3T}$

MCQ 5.130

The K -map for a Boolean function is shown in the figure is the number of essential prime impicates for this function is





	AB	00	01	11	10
CD	00	1	1		1
	01				1
	11	1			
	10	1			1

- (A) 4 (B) 5
(C) 6 (D) 8

1997

ONE MARK

MCQ 5.131

Each cell of a static Random Access Memory contains

- (A) 6 MOS transistors
(B) 4 MOS transistors and 2 capacitors
(C) 2 MOS transistors and 4 capacitors
(D) 1 MOS transistors and 1 capacitors

MCQ 5.132

A 2 bit binary multiplier can be implemented using

- (A) 2 inputs ANDs only
(B) 2 input XORs and 4 input AND gates only
(C) Two 2 inputs NORs and one XNO gate
(D) XOR gates and shift registers

MCQ 5.133

In standard TTL, the 'totem pole' stage refers to

- (A) the multi-emitter input stage
(B) the phase splitter
(C) the output buffer
(D) open collector output stage

MCQ 5.134

The inverter 74 ALS04 has the following specifications

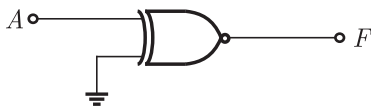
$$I_{OHmax} = -0.4 \text{ A}, I_{OLmax} = 8 \text{ mA}, I_{IHmax} = 20 \text{ mA}, I_{ILmax} = -0.1 \text{ mA}$$

The fan out based on the above will be

- (A) 10 (B) 20
(C) 60 (D) 100

MCQ 5.135

The output of the logic gate in the figure is



- (A) 0 (B) 1
(C) A (D) F

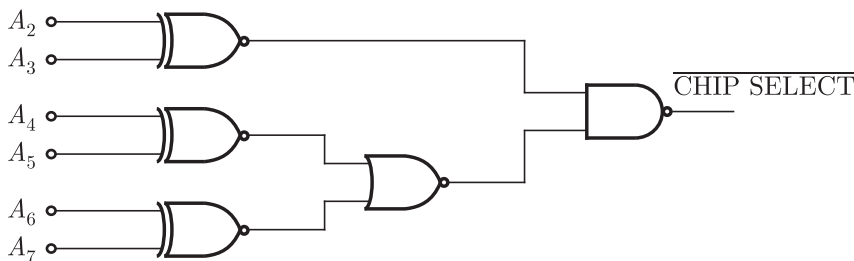
MCQ 5.136

In an 8085 μP system, the RST instruction will cause an interrupt

- (A) only if an interrupt service routine is not being executed
(B) only if a bit in the interrupt mask is made 0
(C) only if interrupts have been enabled by an EI instruction
(D) None of the above

MCQ 5.137

The decoding circuit shown in the figure is has been used to generate the active low chip select signal for a microprocessor peripheral. (The address lines are designated as A_0 to A_7 for I/O address)



The peripheral will correspond to I/O address in the range





- (A) 60 H to 63 H (B) A4 to A 7H
(C) 30 H to 33 H (D) 70 H to 73 H

MCQ 5.138

The following instructions have been executed by an 8085 μ P

ADDRESS (HEX)	INSTRUCTION
6010	LXI H, 8 A 79 H
6013	MOV A, L
6015	ADDH
6016	DAA
6017	MOV H, A
6018	PCHL

From which address will the next instruction be fetched ?

- (A) 6019 (B) 6379
(C) 6979 (D) None of the above

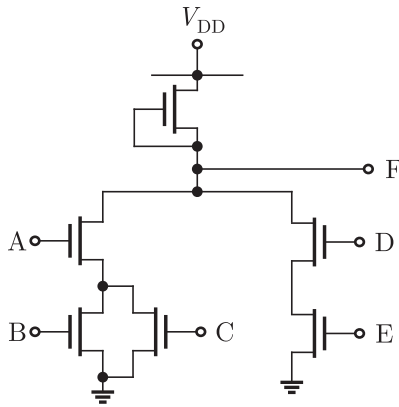
MCQ 5.139

A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should

- (A) copy the original byte to the less significant byte of the word and fill the more significant with zeros
(B) copy the original byte to the more significant byte of the word and fill the less significant byte with zeros
(C) copy the original byte to the less significant byte of the word and make each bit of the more significant byte equal to the most significant bit of the original byte
(D) copy the original byte to the less significant byte as well as the more significant byte of the word

1997**TWO MARKS****MCQ 5.140**

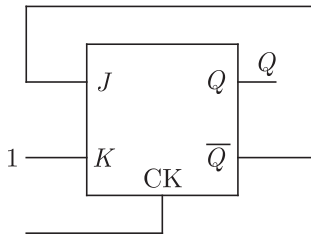
For the NMOS logic gate shown in the figure is the logic function implemented is



- (A) \overline{ABCDE} (B) $(AB + \overline{C}) \cdot (\overline{D} + \overline{E})$
 (C) $\overline{A \cdot (B + C) + D \cdot E}$ (D) $(\overline{A + B}) \cdot C + \overline{D} \cdot \overline{E}$

MCQ 5.141

In a J-K flip-flop we have $J = Q$ and $K = 1$. Assuming the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



- (A) 010000 (B) 011001
 (C) 010010 (D) 010101

MCQ 5.142

The gate delay of an NMOS inverter is dominated by charge time rather than discharge time because

- (A) the driver transistor has larger threshold voltage than the load transistor
 (B) the driver transistor has larger leakage currents compared to the load transistor
 (C) the load transistor has a smaller W/L ratio compared to the driver transistor
 (D) none of the above

**MCQ 5.143**

The boolean function $A + BC$ is a reduced form of

- (A) $AB + BC$ (B) $(A + B) \cdot (A + C)$
(C) $\bar{A}B + A\bar{B}C$ (D) $(A + C) \cdot B$

1996**ONE MARK****MCQ 5.144**

Schottky clamping is resorted in TTL gates

- (A) to reduce propagation delay (B) to increase noise margins
(C) to increase packing density (D) to increase fan-out

MCQ 5.145

A pulse train can be delayed by a finite number of clock periods using

- (A) a serial-in serial-out shift register
(B) a serial-in parallel-out shift register
(C) a parallel-in serial-out shift register
(D) a parallel-in parallel-out shift register

MCQ 5.146

A 12-bit ADC is operating with a $1\mu\text{sec}$ clock period and the total conversion time is seen to be $14\mu\text{sec}$. The ADC must be of the

- (A) flash type (B) counting type
(C) integrating type (D) successive approximation type

MCQ 5.147

The total number of memory accesses involved (inclusive of the op-code fetch) when an 8085 processor executes the instruction LDA 2003 is

- (A) 1 (B) 2
(C) 3 (D) 4

1996

TWO MARKS

MCQ 5.148

A dynamic RAM cell which hold 5 V has to be refreshed every 20 m sec, so that the stored voltage does not fall by more than 0.5 V. If the cell has a constant discharge current of 1 pA, the storage capacitance of the cell is

- (A) 4×10^{-6} F (B) 4×10^{-9} F
(C) 4×10^{-12} F (D) 4×10^{-15} F

MCQ 5.149

A 10-bit ADC with a full scale output voltage of 10.24 V is designed to have a $\pm \text{LSB}/2$ accuracy. If the ADC is calibrated at 25°C and the operating temperature ranges from 0°C to 25°C , then the maximum net temperature coefficient of the ADC should not exceed

- (A) $\pm 200 \mu\text{V}/^\circ\text{C}$ (B) $\pm 400 \mu\text{V}/^\circ\text{C}$
(C) $\pm 600 \mu\text{V}/^\circ\text{C}$ (D) $\pm 800 \mu\text{V}/^\circ\text{C}$

MCQ 5.150

A memory system of size 26 K bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is

- (A) 2 (B) 4
(C) 8 (D) 13

MCQ 5.151

The following sequence of instructions are executed by an 8085 microprocessor:

1000 LXI SP, 27 FF
1003 CALL 1006
1006 POP H

The contents of the stack pointer (SP) and the HL, register pair on completion of execution of these instruction are

- (A) SP = 27 FF, HL = 1003 (B) SP = 27 FD, HL = 1003
(C) SP = 27 FF, HL = 1006 (D) SP = 27 FD, HL = 1006

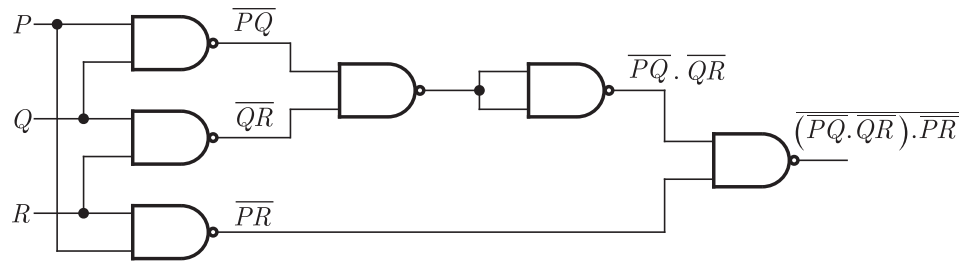




SOLUTIONS

SOL 5.1

The given circuit is shown below:



$$\begin{aligned} \overline{(P\bar{Q} \bar{Q}R) PR} &= \overline{(P\bar{Q} + \bar{Q}R) PR} \\ &= \overline{P\bar{Q} + \bar{Q}R + PR} \\ &= P\bar{Q} + \bar{Q}R + PR \end{aligned}$$

If any two or more inputs are '1' then output y will be 1.
Hence (B) is correct option.

SOL 5.2

For the output to be high, both inputs to AND gate should be high.
The D-Flip Flop output is the same, after a delay.

Let initial input be 0; (Consider Option A)

then $\bar{Q} = 1$ (For 1st D-Flip Flop). This is given as input to 2nd FF.

Let the second input be 1. Now, considering after 1 time interval; The output of 1st Flip Flop is 1 and 2nd FF is also 1. Thus Output = 1.

Hence (A) is correct option.

SOL 5.3

$$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

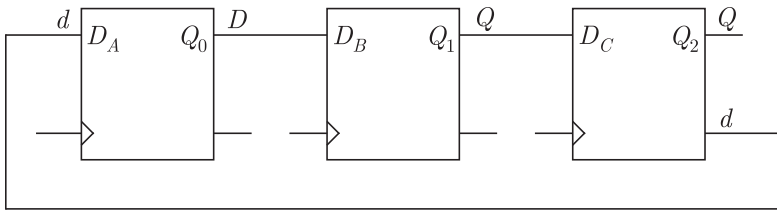
$$I_0 = I_3 = 0$$

$$F = \bar{P}Q + P\bar{Q} = \text{XOR}(P, Q) \quad (S_1 = P, S_0 = Q)$$

Hence (D) is correct option.

SOL 5.4

All the states of the counter are initially unset.



State Initially are shown below in table :

Q_2	Q_1	Q_0	
0	0	0	0
1	0	0	4
1	1	0	6
1	1	1	7
0	1	1	3
0	0	1	1
0	0	0	0

Hence (A) is correct option.

SOL 5.5

The sequence is $Q_B Q_A$

$00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \dots$

Q_B	Q_A	$Q_B(t+1)$	$Q_A(t+1)$
0	0	1	1
1	1	0	1
0	1	1	0
1	0	0	0

$Q_B(t+1)$

	Q_B	0	1
Q_A	0	1	1
	1	0	0

$Q_B(t+1) = \bar{Q}_A$

	Q_B	1	0
Q_A	0	0	1





$$D_A = \overline{Q_A} \overline{Q_B} + Q_A Q_B$$

Hence (D) is correct option.

SOL 5.6

Initially Carry Flag, $C = 0$

MVI A, 07 H ; $A = 0000\ 0111$

RLC ; Rotate left without carry. $A = 0000\ 1110$

MVO B, A ; $B = A = 0000\ 1110$

RLC ; $A = 0001\ 1100$

RLC ; $A = 0011\ 1000$

ADD B ; $A = \begin{array}{r} 0011\ 1000 \\ + 0000\ 1110 \\ \hline 0100\ 0110 \end{array}$

RRC ; Rotate Right with out carry, $A = 0010\ 0011$

Thus $A = 23\ H$

Hence (C) is correct option.

SOL 5.7

$$X \text{---} \overline{X+Y} = \overline{X} \overline{Y} \quad \equiv \quad X \text{---} \overline{X} \overline{Y}$$

$$X \text{---} \overline{X} \overline{Y} = \overline{X} + \overline{Y} \quad \equiv \quad X \text{---} \overline{X} + \overline{Y}$$

$$X \text{---} X \oplus Y = \overline{X} Y + X \overline{Y} \quad \equiv \quad X \text{---} \overline{X} \otimes Y = \overline{X} Y + X \overline{Y}$$

$$X \text{---} X \otimes \overline{Y} = XY + \overline{X} \overline{Y} \quad \equiv \quad X \text{---} X \oplus \overline{Y} = XY + \overline{X} \overline{Y}$$

SOL 5.8

Since $\overline{G_2}$ is active low input, output of NAND gate must be 0

$$\overline{G_2} = \overline{A_{15}} \cdot \overline{A_{14}} \overline{A_{13}} \overline{A_{12}} A_{11} = 0$$

So, $A_{15} A_{14} A_{13} A_{12} A_{11} = 00101$

To select Y_5 Decoder input

$$ABC = A_8 A_9 A_{10} = 101$$

Address range

$A_{15}A_{14}A_{13}A_{12}A_{11}A_{10}A_9A_8\dots\dots\dots A_0$

$\underbrace{001}_2 \underbrace{1101}_D \dots\dots\dots A_0$

$(2D00 - 2DFF)$

Hence (B) is correct option.

SOL 5.9

In the circuit $F = (A \oplus B) \odot (A \odot B) \odot C$

For two variables $A \oplus B = \overline{A \odot B}$

So, $(A \oplus B) \odot (A \odot B) = 0$ (always)

$$F = 0 \odot C = 0 \cdot C + 1 \cdot \overline{C} = \overline{C}$$

So, $F = 1$ when $\overline{C} = 1$ or $C = 0$

Hence (A) (B) (C) are correct options.

SOL 5.10

Let $Q_A(n), Q_B(n), Q_C(n)$ are present states and $Q_A(n+1), Q_B(n+1), Q_C(n+1)$ are next states of flop-flops.

In the circuit

$$Q_A(n+1) = Q_B(n) \odot Q_C(n)$$

$$Q_B(n+1) = Q_A(n)$$

$$Q_C(n+1) = Q_B(n)$$

Initially all flip-flops are reset

1st clock pulse

$$Q_A = 0 \odot 0 = 1$$

$$Q_B = 0$$

$$Q_C = 0$$

2nd clock pulse

$$Q_A = 0 \odot 0 = 1$$

$$Q_B = 1$$

$$Q_C = 0$$

3rd clock pulse

$$Q_A = 1 \odot 0 = 0$$

$$Q_B = 1$$

$$Q_C = 1$$

4th clock pulse

$$Q_A = 1 \odot 1 = 1$$

$$Q_B = 0$$

$$Q_C = 1$$





So, sequence $Q_A = 01101\dots\dots$
Hence (D) is correct option.

SOL 5.11

Output of the MUX can be written as

$$F = I_0 \overline{S_0} \overline{S_1} + I_1 \overline{S_0} S_1 + I_2 S_0 \overline{S_1} + I_3 S_0 S_1$$

Here, $I_0 = C, I_1 = D, I_2 = \overline{C}, I_3 = \overline{CD}$

and $S_0 = A, S_1 = B$

So, $F = C \overline{A} \overline{B} + D \overline{A} B + \overline{C} A \overline{B} + \overline{C} \overline{D} A \overline{B}$

Writing all SOP terms

$$F = \underbrace{\overline{A} \overline{B} C \overline{D}}_{m_3} + \underbrace{\overline{A} \overline{B} C D}_{m_2} + \underbrace{\overline{A} B C D}_{m_7} + \underbrace{\overline{A} B \overline{C} D}_{m_5}$$

$$+ \underbrace{A \overline{B} \overline{C} D}_{m_9} + \underbrace{A \overline{B} C \overline{D}}_{m_8} + \underbrace{A B \overline{C} \overline{D}}_{m_{12}}$$

$$F = \sum m(2, 3, 5, 7, 8, 9, 12)$$

Hence (D) is correct option.

SOL 5.12

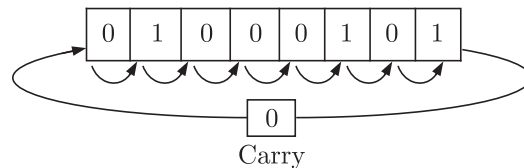
By executing instruction one by one

MVI A, 45 H \Rightarrow MOV 45 H into accumulator, $A = 45$ H

STC \Rightarrow Set carry, $C = 1$

CMC \Rightarrow Complement carry flag, $C = 0$

RAR \Rightarrow Rotate accumulator right through carry



$$A = 00100010$$

XRA B \Rightarrow XOR A and B

$$A = A \oplus B = 00100010 \oplus 01000101 = 01100111 = 67_{16}$$

Hence (C) is correct option.

SOL 5.13

TTL \rightarrow Transistor - Transistor logic

CMOS \rightarrow Complementary Metal Oxide Semi-conductor

Hence (C) is correct answer.

SOL 5.14

Vectored interrupts : Vectored interrupts are those interrupts in which program control transferred to a fixed memory location.

Maskable interrupts : Maskable interrupts are those interrupts which can be rejected or delayed by microprocessor if it is performing some critical task.

Hence (D) is correct answer.

SOL 5.15

We have $[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}][\bar{X} + \bar{Z}(X + Y)] = 1$

Substituting $X = 1$ and $\bar{X} = 0$ we get

$[1 + Z\{\bar{Y} + (\bar{Z} + 1\bar{Y})\}][0 + \bar{Z}(1 + Y)] = 1$

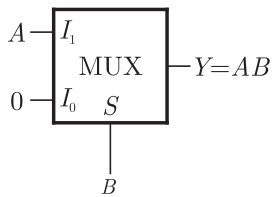
or $[1][\bar{Z}(1)] = 1$ $1 + A = 1$ and $0 + A = A$

or $\bar{Z} = 1 \leftrightarrow Z = 0$

Hence (D) is correct answer.

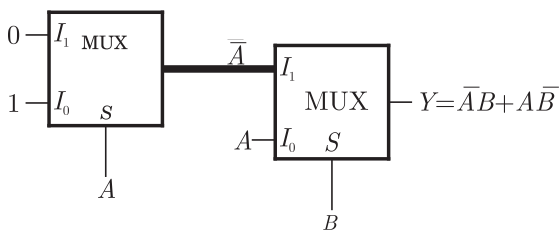
SOL 5.16

The AND gate implementation by 2:1 mux is as follows



$$Y = \bar{A}I_0 + AI_1 = AB$$

The EX-OR gate implementation by 2:1 mux is as follows



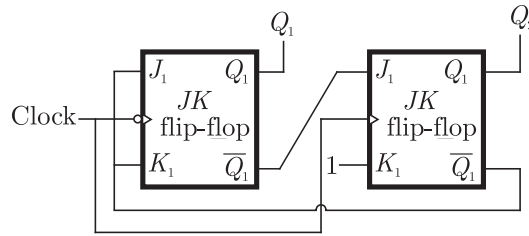
$$Y = \bar{B}I_0 + BI_1 = \bar{A}\bar{B} + A\bar{B}$$

Hence (A) is correct answer.

SOL 5.17

The given circuit is as follows.





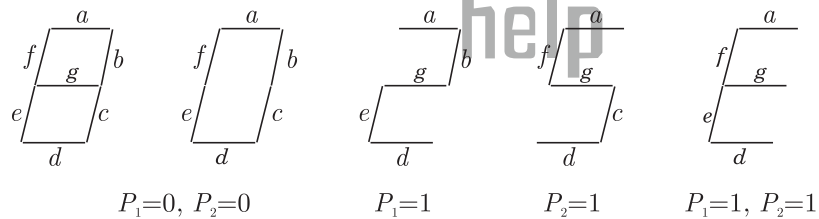
The truth table is as shown below. Sequence is 00, 11, 10, 00 ...

CLK	J_1	K_1	Q_1	J_2	K_2	Q_2
1	1	1	0	1	1	0
2	1	1	1	1	1	1
3	0	0	1	0	1	0
4	1	1	0	1	1	0

Hence (A) is correct answer.

SOL 5.18

The given situation is as follows



The truth table is as shown below

P_1	P_2	a	b	c	d	e	f	g
0	0	1	1	1	1	1	1	0
0	1	1	0	1	1	0	1	1
1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	1	1	1

From truth table we can write

$$\begin{aligned}
 a &= 1 \\
 b &= \overline{P_1} \overline{P_2} + P_1 \overline{P_2} = \overline{P_2} && 1 \text{ NOT Gate} \\
 c &= \overline{P_1} \overline{P_2} + \overline{P_1} P_2 = \overline{P_1} && 1 \text{ NOT Gate} \\
 d &= 1 = c + e
 \end{aligned}$$

and $c = \overline{\overline{P_1} \overline{P_2}} = P_1 + P_2$ 1 OR GATE

$$f = \overline{P_1 P_2} = \overline{P_1} + P_2 \quad 1 \text{ OR GATE}$$

$$g = \overline{\overline{P_1} P_2} = P_1 + P_2 \quad 1 \text{ OR GATE}$$

Thus we have $g = P_1 + P_2$ and $d = 1 = c + e$. It may be observed easily from figure that

Led g does not glow only when both P_1 and P_2 are 0. Thus

$$g = P_1 + P_2$$

LED d is 1 all condition and also it depends on

$$d = c + e$$

Hence (B) is correct answer.

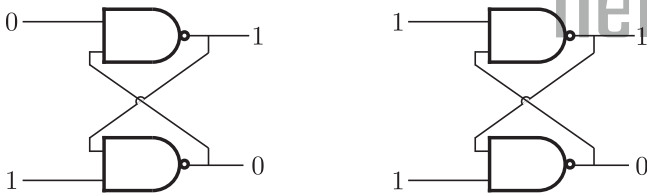
SOL 5.19

As shown in previous solution 2 NOT gates and 3-OR gates are required.

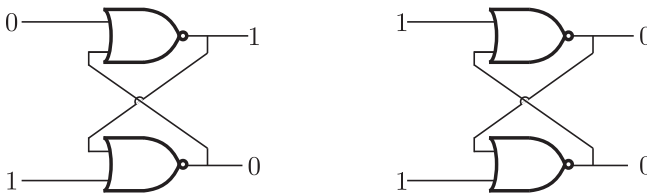
Hence (D) is correct answer.

SOL 5.20

For the NAND latch the stable states are as follows



For the NOR latch the stable states are as follows

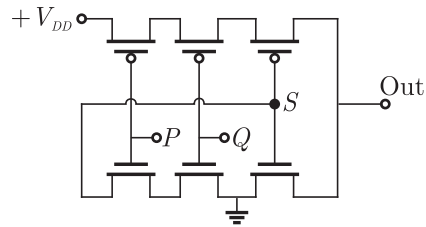


Hence (C) is correct answer.

SOL 5.21

From the figure shown below it may be easily seen upper MOSFET are shorted and connected to V_{dd} thus OUT is 1 only when the node S is 0,





Since the lower MOSFETs are shorted to ground, node S is 0 only when input P and Q are 1. This is the function of AND gate. Hence (D) is correct answer.

SOL 5.22

MSB of both number are 1, thus both are negative number. Now we get

$$11101101 = (-19)_{10}$$

and

$$11100110 = (-26)_{10}$$

$$P - Q = (-19) - (-26) = 7$$

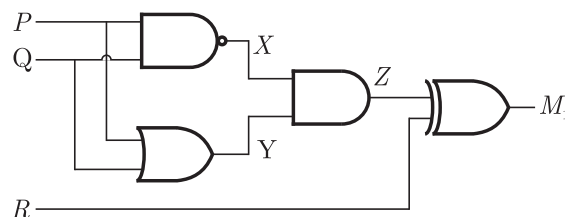
Thus 7 signed two's complements form is

$$(7)_{10} = 00000111$$

Hence (B) is correct answer.

SOL 5.23

The circuit is as shown below



$$X = \overline{PQ}$$

$$Y = (P + Q)$$

So

$$Z = \overline{PQ}(P + Q)$$

$$= (\overline{P} + \overline{Q})(P + Q) = \overline{P}Q + P\overline{Q} = P \oplus Q$$

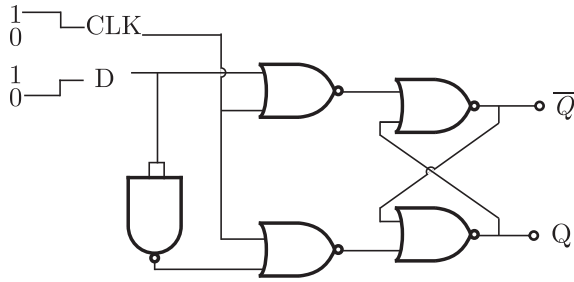
and

$$M_1 = Z \oplus R = (P \oplus Q) \oplus R$$

Hence (D) is correct answer.

SOL 5.24

The circuit is as shown below



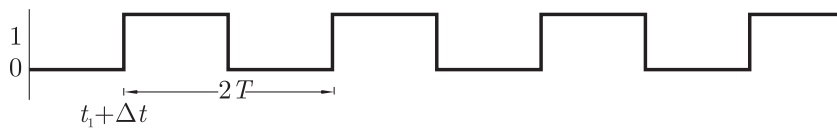
The truth table is shown below. When CLK make transition Q goes to 1 and when D goes to 1, Q goes to 0
Hence (A) is correct answer.

SOL 5.25

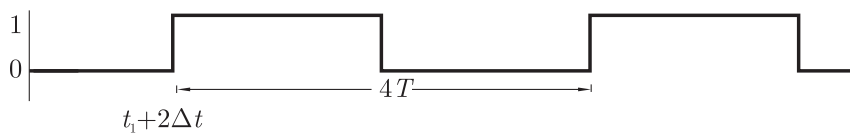
Since the input to both JK flip-flop is 11, the output will change every time with clock pulse. The input to clock is



The output Q_0 of first FF occurs after time ΔT and it is as shown below



The output Q_1 of second FF occurs after time ΔT when it gets input (i.e. after ΔT from t_1) and it is as shown below



Hence (B) is correct answer.

SOL 5.26

We have

$$V_{DAC} = \sum_{n=0}^3 2^{n-1} b_n = 2^{-1} b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3$$

or $V_{DAC} = 0.5b_0 + b_1 + 2b_2 + 4b_3$



The counter outputs will increase by 1 from 0000 till $V_{th} > V_{DAC}$. The output of counter and V_{DAC} is as shown below

Clock	$b_3 b_2 b_1 b_0$	V_{DAC}
1	0001	0
2	0010	0.5
3	0011	1
4	0100	1.5
5	0101	2
6	0110	2.5
7	0111	3
8	1000	3.5
9	1001	4
10	1010	4.5
11	1011	5
12	1100	5.5
13	1101	6
14	1110	6.5

and when $V_{ADC} = 6.5$ V (at 1101), the output of AND is zero and the counter stops. The stable output of LED display is 13.

Hence (D) is correct answer.

SOL 5.27

The $V_{ADC} - V_{in}$ at steady state is

$$= 6.5 - 6.2 = 0.3 V$$

Hence (B) is correct answer.

SOL 5.28

$$\begin{aligned} Z &= I_0 \overline{RS} + I_1 \overline{RS} + I_2 \overline{RS} + I_3 RS \\ &= (P + \overline{Q}) \overline{RS} + \overline{P}RS + PQR\overline{S} + PRS \\ &= \overline{P}RS + \overline{Q}RS + \overline{P}RS + PQR\overline{S} + PRS \end{aligned}$$

The k -Map is as shown below

	RS			
	00	01	11	10
PQ				
00	1			
01				
11	1	1	1	1
10	1	1	1	

$$Z = PQ + P\overline{Q}S + \overline{Q}RS$$

Hence (A) is correct answer.

SOL 5.29

2710H LXI H, 30A0H ; Load 16 bit data 30A0 in HL pair

2713H DAD H ; 6140H → HL

2714H PCHL ; Copy the contents 6140H of HL in PC

Thus after execution above instruction contents of PC and HL are same and that is 6140H

Hence (C) is correct answer.

gate
help

SOL 5.30

MSB of Y is 1, thus it is negative number and X is positive number

Now we have $X = 01110 = (14)_{10}$

and $Y = 11001 = (-7)_{10}$

$$X + Y = (14) + (-7) = 7$$

In signed two's complements from 7 is

$$(7)_{10} = 000111$$

Hence (C) is correct answer.

SOL 5.31

$$Y = AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$$

This is SOP form and we require only 3 NAND gate

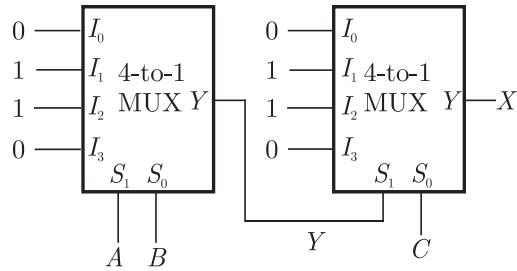
Hence (B) is correct answer.

SOL 5.32

The circuit is as shown below



Chap 5
Digital Circuits



$$Y = \overline{AB} + A\overline{B}$$

and

$$X = \overline{Y}C + Y\overline{C}$$

$$\begin{aligned} &= (\overline{AB} + A\overline{B})C + (\overline{AB} + A\overline{B})\overline{C} \\ &= (\overline{AB} + AB)C + (\overline{AB} + A\overline{B})\overline{C} \\ &= \overline{A}BC + ABC + \overline{A}B\overline{C} + A\overline{B}\overline{C} \end{aligned}$$

Hence (A) is correct answer.

SOL 5.33

$$\begin{aligned} Y &= \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B}C\overline{D} + A\overline{B}CD \\ &= \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B}C\overline{D} + A\overline{B}CD \\ &= \overline{A}BC\overline{D} + \overline{A}BCD + \overline{B}CD(A + \overline{A}) \\ &= \overline{A}BC\overline{D} + \overline{A}BCD + \overline{B}CD \end{aligned}$$

$$A + \overline{A} = 1$$

Hence (D) is correct answer.

SOL 5.34

In given TTL NOT gate when $V_i = 2.5$ (HIGH), then

- $Q_1 \rightarrow$ Reverse active
- $Q_2 \rightarrow$ Saturation
- $Q_3 \rightarrow$ Saturation
- $Q_4 \rightarrow$ cut - off region

Hence (B) is correct answer.

SOL 5.35

- For $X = 0, Y = 1$ $P = 1, Q = 0$
- For $X = 0, Y = 0$ $P = 1, Q = 1$
- For $X = 1, Y = 1$ $P = 1, Q = 0$ or $P = 0, Q = 1$

Hence (C) is correct answer.

SOL 5.36

Chip 8255 will be selected if bits A_3 to A_7 are 1. Bit A_0 to A_2 can be 0 or.

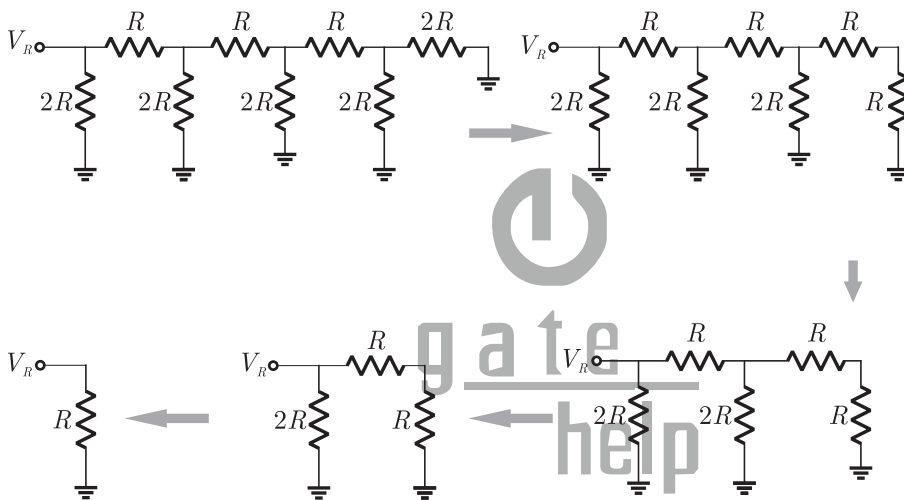
1. Thus address range is

$$\begin{array}{ll} 11111000 & \text{F8H} \\ 11111111 & \text{FFH} \end{array}$$

Hence (C) is correct answer.

SOL 5.37

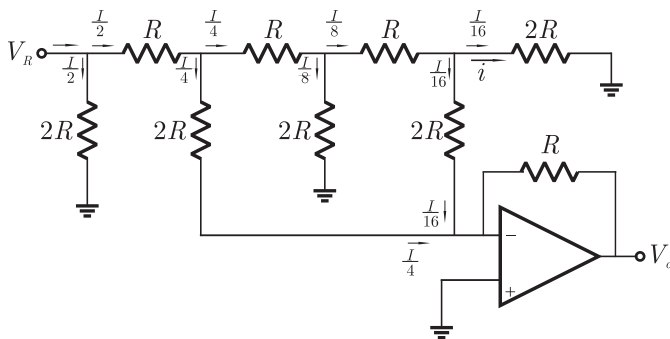
Since the inverting terminal is at virtual ground the resistor network can be reduced as follows



The current from voltage source is

$$I = \frac{V_R}{R} = \frac{10}{10k} = 1 \text{ mA}$$

This current will be divide as shown below



Now
$$i = \frac{I}{16} = \frac{1 \times 10^{-3}}{16} = 62.5 \mu \text{ A}$$

Hence (B) is correct answer.





SOL 5.38

The net current in inverting terminal of OP - amp is

$$I = \frac{1}{4} + \frac{1}{16} = \frac{5I}{16}$$

So that $V_0 = -R \times \frac{5I}{16} = -3.125$

Hence (C) is correct answer.

SOL 5.39

Line 1 : MVI A, B5H ; Move B5H to A
 2 : MVI B, 0EH ; Move 0EH to B
 3 : XRI 69H ; [A] XOR 69H and store in A
 ; Contents of A is CDH
 4 : ADDB ; Add the contents of A to contents of B and
 ; store in A, contents of A is EAH
 5 : ANI 9BH ; [a] AND 9BH, and store in A,
 ; Contents of A is 8 AH
 6 : CPI 9FH ; Compare 9FH with the contents of A
 ; Since 8 AH < 9BH, CY = 1
 7 : STA 3010 H ; Store the contents of A to location 3010 H
 8 : HLT ; Stop

Thus the contents of accumulator after execution of ADD instruction is EAH.

Hence (B) is correct answer.

SOL 5.40

The $CY = 1$ and $Z = 0$
 Hence (C) is correct answer.

SOL 5.41

For this circuit the counter state (Q_1, Q_0) follows the sequence 00, 01, 10, 00 ... as shown below

Clock	$D_1 D_0$	$Q_1 Q_0$	$Q_1 \text{ NOR } Q_0$
		00	1
1st	01	10	0
2nd	10	01	0
3rd	00	00	0

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

Hence (A) is correct answer.

SOL 5.42

As shown below there are 2 terms in the minimized sum of product expression.

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

Hence (A) is correct answer.



SOL 5.43

The output is taken from the 5th line.
Hence (B) is correct answer.

SOL 5.44

After applying two clock poles, the outputs of the full adder is $S = 1$, $C_0 = 1$

	A	B	C_i	S	C_o
1st	1	0	0	0	1
2nd	1	1	1	1	1

Hence (D) is correct answer.

SOL 5.45

100010011001
4 2 3 1

Hence (D) is correct answer.

SOL 5.46

In this the diode D_2 is connected to the ground. The following table





shows the state of counter and D/A converter

$Q_2 Q_1 Q_0$	$D_3 = Q_2$	$D_2 = 0$	$D_1 = Q_1$	$D_0 = Q_0$	V_o
000	0	0	0	0	0
001	0	0	0	1	1
010	0	0	1	0	2
011	0	0	1	1	3
100	1	0	0	0	8
101	1	0	0	1	9
110	1	0	1	0	10
111	1	0	1	1	11
000	0	0	0	0	0
001	0	0	0	1	1

Thus option (B) is correct

SOL 5.47

```
LXI, EFFF H           ; Load SP with data EFFFH
CALL 3000 H          ; Jump to location 3000 H
:
:
:
3000H LXI H, 3CF4    ; Load HL with data 3CF4H
PUSH PSW             ; Store contents of PSW to Stack
POP PSW              ; Restore contents of PSW from stack
PRE                   ; stop
```

Before instruction SPHL the contents of SP is 3CF4H.

After execution of POP PSW, $SP + 2 \rightarrow SP$

After execution of RET, $SP + 2 \rightarrow SP$

Thus the contents of SP will be $3CF4H + 4 = 3CF8H$

Hence (B) is correct answer.

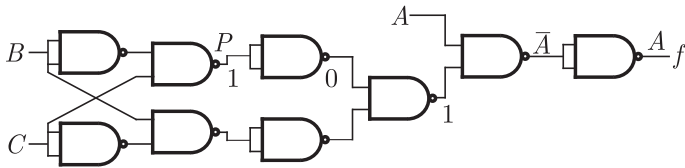
SOL 5.48

The inputs D_0 and D_1 respectively should be connected as $\overline{Q_1}$ and Q_0 where $Q_0 \rightarrow D_1$ and $\overline{Q_1} \rightarrow D_0$

Hence (A) is correct answer.

SOL 5.49

If the point P is stuck at 1, then output f is equal to A



Hence (D) is correct answer.

SOL 5.50

Dividing 43 by 16 we get

$$\begin{array}{r} 2 \\ 16 \overline{)43} \\ \underline{32} \\ 11 \end{array}$$

11 in decimal is equivalent is B in hexamal.

Thus $43_{10} \leftrightarrow 2B_{16}$

Now $4_{10} \leftrightarrow 0100_2$

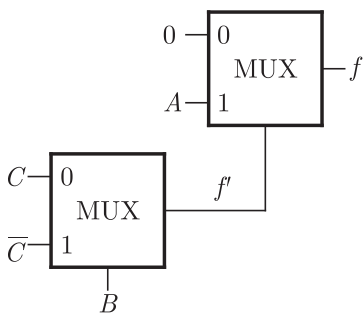
$3_{10} \leftrightarrow 0011_2$

Thus $43_{10} \leftrightarrow 01000011_{BCD}$

Hence (B) is correct answer.

SOL 5.51

The diagram is as shown in fig



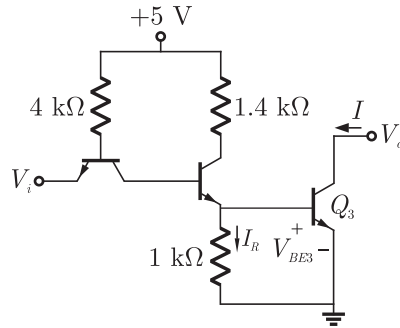
$$\begin{aligned} f &= B\bar{C} + \bar{B}C \\ f &= fA + \bar{f}0 \\ &= fA = ABC\bar{C} + A\bar{B}C \end{aligned}$$

Hence (A) is correct answer.



**SOL 5.52**

The circuit is as shown below



If output is at logic 0, then we have $V_o = 0$ which signifies BJT Q_3 is in saturation and applying KVL we have

$$V_{BE3} = I_R \times 1k$$

or $0.75 = I_R \times 1k$

or $I_R = 0.75 \text{ mA}$

Hence (C) is correct answer.

SOL 5.53

We have

$$\begin{aligned} f &= ABC + \bar{A}BC \\ &= B(\bar{A}C + AC) = B(A + \bar{A})(\bar{A} + C) \end{aligned}$$

Hence (A) is correct answer.

SOL 5.54

Characteristic equation for a jk flip-flop is written as

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Where Q_n is the present output

Q_{n+1} is next output

So, $Q_{n+1} = 1\bar{0} + \bar{K} \cdot 0$

$$Q_n = 0$$

$$Q_{n+1} = 1$$

Hence (C) is correct answer.

SOL 5.55

Since $T_2 T_1 T_0$ is at 111, at every clock $Q_2 Q_1 Q_0$ will be changes. In present state is 011, the next state will be 100.

Hence (C) is correct answer.

SOL 5.56

Hence (D) is correct answer.

SOL 5.57

```

0100H LXI SP, 00FF      ; Load SP with 00FFH
0103H LXI H, 0701       ; Load HL with 0107H
0106H MVI A, 20H        ; Move A with 20H
0108H SUB M              ; Subtract the contents of memory
                          ; location whose address is stored in HL
                          ; from the A and store in A
0109H ORI 40H           ; 40H OR [A] and store in A
010BH ADD M              ; Add the contents of memory location
                          ; whose address is stored in HL to A
                          ; and store in A

```

HL contains 0107H and contents of 0107H is 20H

Thus after execution of SUB the data of A is $20H - 20H = 00$

Hence (C) is correct answer.

SOL 5.58

Before ORI instruction the contents of A is 00H. On execution the ORI 40H the contents of A will be 40H

$$00H = 00000000$$

$$40H = 01000000$$

$$\text{ORI } 01000000$$

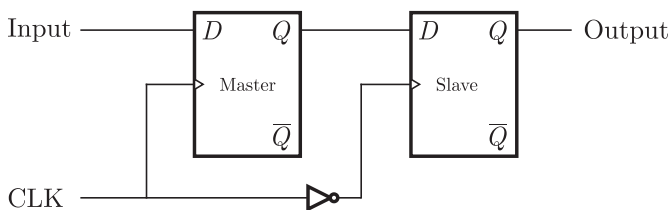
After ADD instruction the contents of memory location whose address is stored in HL will be added to and will be stored in A

$$40H + 20H = 60H$$

Hence (C) is correct answer.

SOL 5.59

A master slave D-flip flop is shown in the figure.



In the circuit we can see that output of flip-flop can be triggered only by transition of clock from 1 to 0 or when state of slave latch is affected.

Hence (C) is correct answer.



**SOL 5.60**

The range of signed decimal numbers that can be represented by n – bits 1's complement number is $-(2^{n-1} - 1)$ to $+(2^{n-1} - 1)$.

Thus for $n = 6$ we have

$$\begin{aligned}\text{Range} &= -(2^{6-1} - 1) \text{ to } +(2^{6-1} - 1) \\ &= -31 \text{ to } +31\end{aligned}$$

Hence (A) is correct answer.

SOL 5.61

The minimum number of bit require to encode 100 increment is

$$2^n \geq 100$$

or $n \geq 7$

Hence (D) is correct answer.

SOL 5.62

Shift Register → Serial to parallel data conversion

Counter → Frequency division

Decoder → Addressing in memory chips.

Hence (B) is correct answer.

SOL 5.63

For the TTL family if terminal is floating, then it is at logic 1.

Thus $Y = (\overline{AB + 1}) = \overline{AB}.0 = 0$

Hence (A) is correct answer.

SOL 5.64

11001	1001	111001
00110	0110	000110
+1	+1	+1
<u>00111</u>	<u>0111</u>	<u>000111</u>
7	7	7

Thus 2's complement of 11001, 1001 and 111001 is 7. So the number given in the question are 2's complement correspond to -7.

Hence (C) is correct answer.

SOL 5.65

In the modulo - 6 ripple counter at the end of sixth pulse (i.e. after

101 or at 110) all states must be cleared. Thus when CB is 11 the all states must be cleared. The input to 2-input gate is \overline{C} and \overline{B} and the desired output should be low since the CLEAR is active low
Thus when \overline{C} and \overline{B} are 0, 0, then output must be 0. In all other case the output must be 1. OR gate can implement this functions.
Hence (C) is correct answer.

SOL 5.66

Number of MUX is $\frac{4}{3} = 2$ and $\frac{2}{2} = 1$. Thus the total number 3 multiplexers is required.
Hence (C) is correct answer.

SOL 5.67

$$\begin{aligned} AC + B\overline{C} &= AC1 + B\overline{C}1 \\ &= AC(B + \overline{B}) + B\overline{C}(A + \overline{A}) \\ &= ACB + AC\overline{B} + B\overline{C}A + B\overline{C}\overline{A} \end{aligned}$$

Hence (D) is correct answer.

SOL 5.68

We have $f(x, y) = \overline{\overline{xy}} + \overline{\overline{xy}} + xy = \overline{x(y+y)} + xy = \overline{x} + xy$
or $f(x, y) = \overline{x} + y$

Here compliments are not available, so to get \overline{x} we use NOR gate.
Thus desired circuit require 1 unit OR and 1 unit NOR gate giving total cost 2 unit.

Hence (D) is correct answer.

SOL 5.69

For 8255, various modes are described as following.

Mode 1 : Input or output with hand shake

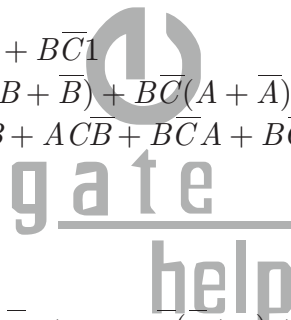
In this mode following actions are executed

1. Two port (A & B) function as 8 - bit input output ports.
2. Each port uses three lines from C as a hand shake signal
3. Input & output data are latched.

Form (ii) the mode is 1.

Mode 2 : Bi-directional data transfer

This mode is used to transfer data between two computer. In this mode port A can be configured as bidirectional port. Port A uses five





signal from port C as hand shake signal.

For (1), mode is 2

Hence (D) is correct answer.

SOL 5.70

LDA 16 bit \Rightarrow Load accumulator directly this instruction copies data byte from memory location (specified within the instruction) the accumulator.

It takes 4 memory cycle-as following.

1. in instruction fetch
2. in reading 16 bit address
1. in copying data from memory to accumulator

LXI D, (F0F1)₄ \Rightarrow It copies 16 bit data into register pair D and E.

It takes 3 memory cycles.

Hence (B) is correct answer.

SOL 5.71

```
LXI H, 9258H      ; 9258H  $\rightarrow$  HL
MOV A, M          ; (9258H)  $\rightarrow$  A
CMa               ;  $\bar{A} \rightarrow A$ 
MOV M, A          ; A  $\rightarrow$  M
```

This program complement the data of memory location 9258H.

Hence (A) is correct answer.

SOL 5.72

```
MVI A, 00H        ; Clear accumulator
LOOP ADD B        ; Add the contents of B to A
DCR C             ; Decrement C
JNZ LOOP         ; If C is not zero jump to loop
HLT
END
```

This instruction set add the contents of B to accumulator to contents of C times.

Hence (D) is correct answer.

SOL 5.73

The number of distinct boolean expression of n variable is 2^{2^n} . Thus

$$2^{2^4} = 2^{16} = 65536$$

Hence (D) is correct answer.

SOL 5.74

In the flash analog to digital converter, the no. of comparators is equal to 2^{n-1} , where n is no. of bit.s

So,
$$2^{n-1} = 2^8 - 1 = 255$$

Hence (C) is correct answer.

SOL 5.75

When output of the 74 series gate of TTL gates is taken from BJT then the configuration is either totem pole or open collector configuration .

Hence (B) is correct answer.

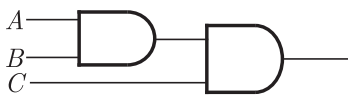
SOL 5.76

A $2^n:1$ MUX can implement all logic functions of $(n+1)$ variable without any additional circuitry. Here $n=3$. Thus a $8:1$ MUX can implement all logic functions of 4 variable.

Here (D) is correct answer.

SOL 5.77

Counter must be reset when it count 111. This can be implemented by following circuitry



Hence (D) is correct answer.

SOL 5.78

We have
$$Y = P \oplus Q \oplus R$$
$$Z = RQ + \bar{P}R + Q\bar{P}$$

Here every block is a full subtractor giving $P - Q - R$ where R is borrow. Thus circuit acts as a 4 bit subtractor giving $P - Q$.

Hence (B) is correct answer.



**SOL 5.79**

$$\begin{aligned}
 W &= R + \overline{P}Q + \overline{R}S \\
 X &= P\overline{Q}RS + \overline{P}QR\overline{S} + P\overline{Q}R\overline{S} \\
 Y &= RS + \overline{P}R + \overline{P}Q + \overline{P}\overline{Q} \\
 &= RS + \overline{P}R \cdot \overline{P}\overline{Q} \cdot \overline{P}\overline{Q} \\
 &= RS + (\overline{P} + \overline{R})(\overline{P} + \overline{Q})(P + Q) \\
 &= RS + (\overline{P} + \overline{P}Q + \overline{P}R + \overline{Q}\overline{R})(P + Q) \\
 &= RS + \overline{P}Q + \overline{Q}\overline{R}(P + \overline{P}) + \overline{Q}\overline{R} \\
 &= RS + \overline{P}Q + \overline{Q}\overline{R} \\
 Z &= R + S + \overline{P}Q + \overline{P}Q\overline{R} + P\overline{Q}S \\
 &= R + S + \overline{P}Q \cdot \overline{P}Q\overline{R} \cdot P\overline{Q}S \\
 &= R + S + (\overline{P} + \overline{Q})(P + Q + R)(\overline{P} + Q + S) \\
 &= R + S + \overline{P}Q + \overline{P}Q + \overline{P}Q\overline{R} + \overline{P}R + \overline{P}QR \\
 &\quad + \overline{P}RS + P\overline{Q} + P\overline{Q}S + \overline{P}Q\overline{R} + \overline{Q}RS \\
 &= R + S + \overline{P}Q + \overline{P}Q\overline{R} + \overline{P}R + \overline{P}QR + \overline{P}RS \\
 &\quad + P\overline{Q}S + \overline{P}Q\overline{R} + \overline{Q}RS \\
 &= R + S + \overline{P}Q(1 + \overline{R}) + \overline{P}R(1 + \overline{Q}) + \overline{P}RS \\
 &\quad + P\overline{Q}S + \overline{P}Q\overline{R} + \overline{Q}RS \\
 &= R + S + \overline{P}Q + \overline{P}R + \overline{P}RS + P\overline{Q}S \\
 &\quad + \overline{P}Q\overline{R} + \overline{Q}RS \\
 &= R + S + \overline{P}Q + \overline{P}R(1 + \overline{Q}) + P\overline{Q}S + \overline{Q}RS \\
 &= R + S + \overline{P}Q + \overline{P}R + P\overline{Q}S + \overline{Q}RS
 \end{aligned}$$

Thus $W = Z$ and $X = \overline{Z}$

Hence (A) is correct answer.

SOL 5.80

Propagation delay of flip flop is

$$t_{pd} = 10 \text{ nsec}$$

Propagation delay of 4 bit ripple counter

$$R = 4t_{pd} = 40 \text{ ns}$$

and in synchronous counter all flip-flop are given clock simultaneously, so

$$S = t_{pd} = 10 \text{ ns}$$

Hence (B) is correct answer.

SOL 5.81

After $t = t_1$, at first rising edge of clock, the output of shift register is 0110, which in input to address line of ROM. At 0110 is applied to

register. So at this time data stored in ROM at 1010 (10), 1000 will be on bus.

When W has the data 0110 and it is 6 in decimal, and its data value at that add is 1010

then 1010 i.e. 10 is acting as odd, at time t_2 and data at that movement is 1000.

Hence (C) is correct answer.

SOL 5.82

The DTL has minimum fan out and CMOS has minimum power consumption. Propagation delay is minimum in ECL.

Hence (B) is correct answer.

SOL 5.83

Let input be 1010; output will be 1101

Let input be 0110; output will be 0100

Thus it convert gray to Binary code.

Hence (D) is correct answer.

SOL 5.84

CMP B \Rightarrow Compare the accumulator content with context of Register B

If $A < R$ CY is set and zero flag will be reset.

Hence (A) is correct answer.

SOL 5.85

$$V_o = -V_1 \left[\frac{R}{R} b_0 + \frac{R}{2R} b_1 + \frac{R}{4R} b_2 + \frac{R}{4R} b_3 \right]$$

Exact value when $V_1 = 5$, for maximum output

$$V_{oExact} = -5 \left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \right] = -9.375$$

Maximum V_{out} due to tolerance

$$\begin{aligned} V_{o\max} &= -5.5 \left[\frac{110}{90} + \frac{110}{2 \times 90} + \frac{110}{4 \times 90} + \frac{110}{8 \times 90} \right] \\ &= -12.604 \end{aligned}$$

Tolerance = 34.44% = 35%

Hence (A) is correct answer.



**SOL 5.86**

If the 4-bit 2's complement representation of a decimal number is 1000, then the number is -8
Hence (D) is correct answer.

SOL 5.87

Output of 1st XOR = $\bar{X} \cdot 1 + X \cdot \bar{1} = \bar{X}$

Output of 2nd XOR = $\overline{\bar{X}X} + XX = 1$

So after 4,6,8,...20 XOR output will be 1.

Hence (B) is correct answer.

SOL 5.88

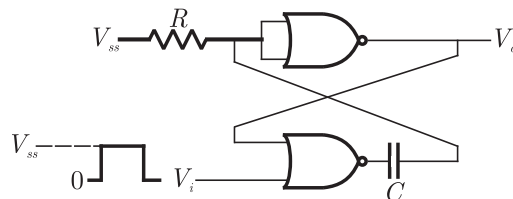
In the comparator type ADC, the no. of comparators is equal to 2^{n-1} , where n is no. of bits

So, $2^3 - 1 = 7$

Hence (C) is correct answer.

SOL 5.89

The circuit is as shown below



The circuit shown is monostable multivibrator as it requires an external triggering and it has one stable and one quasistable state.

Hence (C) is correct answer.

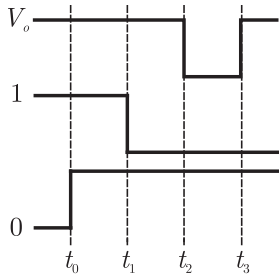
SOL 5.90

They have propagation delay as respectively,

$$G_1 \rightarrow 10 \text{ nsec}$$

$$G_2 \rightarrow 20 \text{ nsec}$$

For abrupt change in V_i from 0 to 1 at time $t = t_0$ we have to assume the output of NOR then we can say that option (B) is correct waveform.



Hence (B) is correct answer.

SOL 5.91

Let $X_3X_2X_1X_0$ be 1001 then $Y_3Y_2Y_1Y_0$ will be 1111.

Let $X_3X_2X_1X_0$ be 1000 then $Y_3Y_2Y_1Y_0$ will be 1110

Let $X_3X_2X_1X_0$ be 0110 then $Y_3Y_2Y_1Y_0$ will be 1100

So this converts 2-4-2-1 BCD numbers.

Hence (B) is correct answer.

SOL 5.92

```

                MVI B, 87H      ; B = 87
                MOV A, B        ; A = B = 87
START :        JMP NEXT       ; Jump to next
                XRA B           ; A ⊕ B → A,
                                ; A = 00, B = 87
                JP START       ; Since A = 00 is positive
                                ; so jump to START
                JMP NEXT       ; Jump to NEXT ; unconditionally
NEXT :        XRA              ; B ; A ⊕ B → A, A = 87,
                                ; B = 87 H
                JP START       ; will not jump as D7, of A is 1
                OUT PORT2      ; A = 87 → PORT2

```

Hence (B) is correct answer.

SOL 5.93

The two's complement representation of 17 is

$$17 = 010001$$

Its 1's complement is 101110

So 2's complement is

$$\begin{array}{r} 101110 \\ + 1 \\ \hline 101111 \end{array}$$

Hence (B) is correct answer.



**SOL 5.94**

The propagation delay of each inverter is t_{pd} then The fundamental frequency of oscillator output is

$$f = \frac{1}{2nt_{pd}} = \frac{1}{2 \times 5 \times 100 \times 10^{-12}} = 1 \text{ GHz}$$

Hence (C) is correct answer.

SOL 5.95

$4K \times 8$ bit means 1024_{10} location of byte are present

Now $1024_{10} \leftrightarrow 1000_H$

It starting address is $AA00_H$ then address of last byte is

$$AA00_H + 1000_H - 0001_H = B9FF_H$$

Hence (C) is correct answer.

SOL 5.96

$$\begin{aligned} Y &= I_0 + I_3 + I_5 + I_6 \\ &= \overline{C}BA + C\overline{A}B + C\overline{B}A + C\overline{B}\overline{A} \\ &= \overline{C}(\overline{B}A + AB) + C(\overline{A}B + \overline{B}\overline{A}) \end{aligned}$$

or
$$Y = \overline{C}(A \oplus B) + C(A \oplus \overline{B})$$

Hence (D) is correct answer.

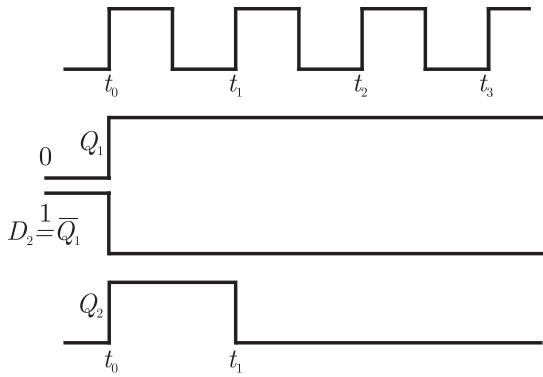
SOL 5.97

For the LED to glow it must be forward biased. Thus output of NAND must be LOW for LED to emit light. So both input to NAND must be HIGH. If any one or both switch are closed, output of AND will be LOW. If both switch are open, output of XOR will be LOW. So there can't be both input HIGH to NAND. So LED doesn't emit light.

Hence (D) is correct answer.

SOL 5.98

The output of options (C) satisfy the given conditions



Hence (C) is correct answer.

SOL 5.99

Hence (B) is correct answer.

SOL 5.100

Conversion time of successive approximate analog to digital converters is independent of input voltage. It depends upon the number of bits only. Thus it remains unchanged.

Hence (B) is correct answer.

SOL 5.101

In the flash analog to digital converter, the no. of comparators is equal to 2^{n-1} , where n is no. of bits.

So, $2^4 - 1 = 15$

Hence (C) is correct answer.

SOL 5.102

As the output of AND is $X = 1$, the all input of this AND must be 1. Thus

$$\overline{A}B + A\overline{B} = 1 \quad \dots(1)$$

$$\overline{B}C + B\overline{C} = 1 \quad \dots(2)$$

$$C = 1 \quad \dots(3)$$

From (2) and (3), if $C = 1$, then $B = 1$

If $B = 1$, then from (1) $A = 0$. Thus $A = 0, B = 1$ and $C = 1$

Hence (D) is correct answer.



**SOL 5.103**

Interrupt is a process of data transfer by which an external device can inform the processor that it is ready for communication. 8085 microprocessor have five interrupts namely TRAP, INTR, RST 7.5, RST 6.5 and RST 5.5

Hence (C) is correct answer.

SOL 5.104

For any RST instruction, location of program transfer is obtained in following way.

RST $x \Rightarrow (x * 8)_{10} \rightarrow$ convert in hexadecimal

So for RST 6 $\Rightarrow (6 * 8)_{10} = (48)_{10} = (30)_H$

Hence (A) is correct answer.

SOL 5.105

Accumulator contains $A = 49 H$

Register $B = 3 AH$

SUB $B = A$ minus B

$A = 49 H = 01001001$

$B = 3 AH = 00111010$

2's complement of $(-B) = 11000110$

$A - B = A + (-B)$

01001001

$\Rightarrow \underline{+11000110}$

00001111

Carry = 1

so here output $A = 0 F$

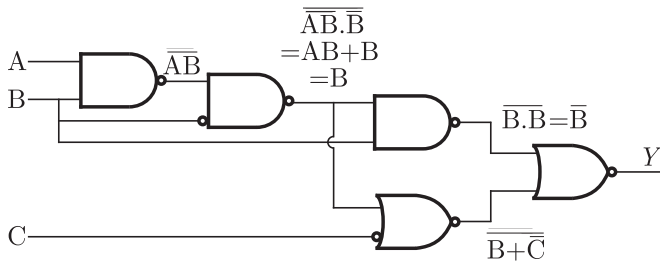
Carry $CY = 1$

Sign flag $S = 1$

Hence (A) is correct answer.

SOL 5.106

The circuit is as shown below :

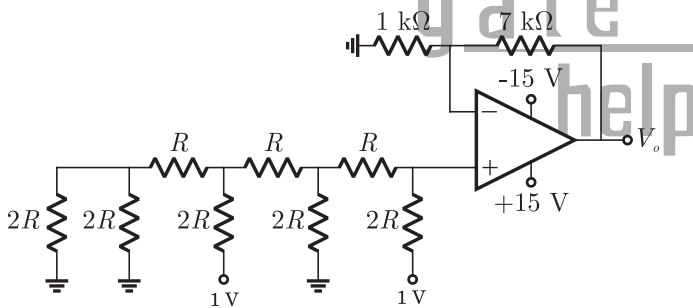


$$Y = \overline{B} + (\overline{B + C}) = B(B + \overline{C}) = B$$

Hence (C) is correct answer.

SOL 5.107

The circuit is as shown below



The voltage at non-inverting terminal is

$$V_+ = \frac{1}{8} + \frac{1}{2} = \frac{5}{8}$$

$$V_o = V_+ = \frac{5}{8} \quad \dots(1)$$

Now applying voltage divider rule

$$V_o = \frac{1k}{1k + 7k} V_o = \frac{1}{8} V_o \quad \dots(2)$$

From (1) and (2) we have

$$V_o = 8 \times \frac{5}{8} = 5V$$

Hence (B) is correct answer.



**SOL 5.108**

The truth table is shown below

$$Z = \overline{X}Q + Y\overline{Q}$$

Comparing from the truth table of $J-K$ FF

$$Y = J,$$

$$X = K$$

X	Y	Z
0	0	Q
0	1	0
1	0	1
1	1	\overline{Q}_1

Hence (D) is correct answer.

SOL 5.109

In the figure the given counter is mod-10 counter, so frequency of output is $\frac{10k}{10} = 1k$

Hence (B) is correct answer.

SOL 5.110

We have $y = A + \overline{A}B$

we know from Distributive property

$$x + yz = (x + y)(x + z)$$

$$\begin{aligned} \text{Thus } y &= (A + \overline{A})(A + B) \\ &= A + B \end{aligned}$$

$$\therefore A + \overline{A} = 1$$

Hence (D) is correct answer.

SOL 5.111

Darlington emitter follower provides a low output impedance in both logical state (1 or 0). Due to this low output impedance, any stray capacitance is rapidly charged and discharged, so the output state changes quickly. It improves speed of operation.

Hence (C) is correct answer.

SOL 5.112

Hence (D) is correct answer.

SOL 5.113

For ADC we can write

$$\text{Analog input} = (\text{decimal eq of digital output}) \times \text{resol}$$

$$6.6 = (\text{decimal eq. of digital output}) \times 0.5$$

$$\frac{6.6}{0.5} = \text{decimal eq of digital. output}$$

$$13.2 = \text{decimal equivalent of digital output so output}$$

of ADC is = 1101.

Hence (B) is correct answer.

SOL 5.114

We use the *K*-map as below.

	BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
\overline{A}	1		1	1	
A				1	



So given expression equal to

$$= \overline{A}\overline{C} + B\overline{C} + \overline{A}B$$

Hence (A) is correct answer.

SOL 5.115

For a binary half-subtractor truth table si given below.

A	B	$D = A \text{ minus } B$	Borrow (X)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

from truth table we can find expressions of D & X

$$D = A \oplus B = \overline{A}B + A\overline{B}$$

$$X = \overline{A}B$$

Hence (C) is correct answer.





SOL 5.116

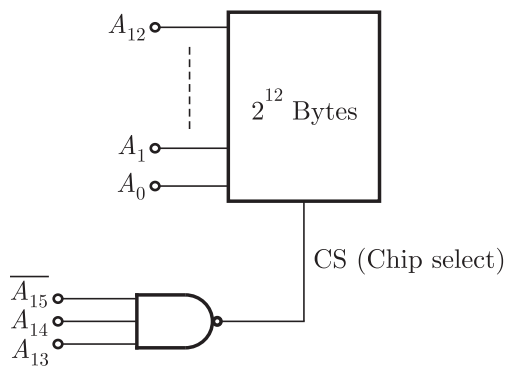
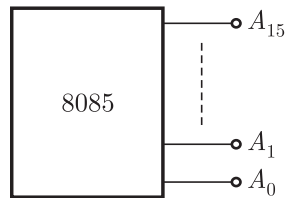
From the given figure we can write the output

Q_A	Q_B	Q_C
1	1	1
0	1	1
1	0	1
0	0	1
1	1	0
0	1	0

For the state 010 all preset = 1 and output $Q_A Q_B Q_C = 111$ so here total no. of states = 5 (down counter)
Hence (D) is correct answer.

SOL 5.117

We have 4 K RAM (12 address lines)



so here chip select logic $CS = A_{15} A_{14} A_{13}$

address range (111)

initial $A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$
 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

address $\Rightarrow 7\ 0\ 0\ 0\ H$
 final $1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
 address $\Rightarrow 7\ F\ F\ F\ H$
 so address range is $(7\ 0\ 0\ 0\ H - 7\ F\ F\ F\ H)$
 Hence (B) is correct answer.

SOL 5.118

Given boolean function is

$$Z = A\bar{B}C$$

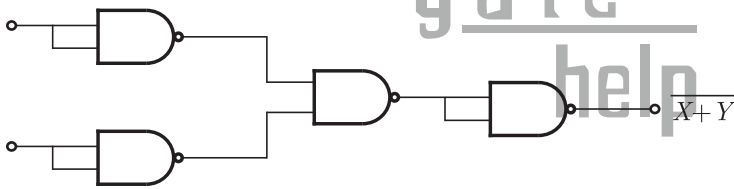
Now $\bar{Z} = \overline{A\bar{B}C} = \overline{A}CB = \overline{A}C + B$

Thus $Z = \overline{\overline{A}C + B}$

we have $Z = \overline{X + Y}$ (1 NOR gate)

where $X = \overline{A}C$ (1 NAND gate)

To implement a NOR gate we required 4 NAND gates as shown below in figure.



here total no. of NAND gates required
 $= 4 + 1 = 5$

Hence (C) is correct answer.

SOL 5.119

For TTL worst cases low voltages are

$$V_{OL}(\max) = 0.4\ V$$

$$V_{IL}(\max) = 0.8\ V$$

Worst case high voltages are

$$V_{OH}(\min) = 2.4\ V$$

$$V_{IH}(\min) = 2\ V$$

The difference between maximum input low voltage and maximum output low voltage is called noise margin. It is 0.4 V in case of TTL.

Hence (B) is correct answer.



**SOL 5.120**

From the figure we can see

If $A = 1$ $B = 0$

then $y = 1$ $x = 0$

If $A = 1$ $B = 1$

then also $y = 1$ $x = 0$

so for sequence $B = 101010\dots$ output x and y will be fixed at 0 and 1 respectively.

Hence (D) is correct answer.

SOL 5.121

Given 2's complement no. 1101; the no. is 0011

for 6 digit output we can write the no. is - 000011

2's complement representation of above no. is 111101

Hence (D) is correct answer.

SOL 5.122

Hence (A) is correct answer.

SOL 5.123

An *I/O* Microprocessor controls data flow between main memory and the *I/O* device which wants to communicate.

Hence (B) is correct answer.

SOL 5.124

Hence (D) is correct answer.

SOL 5.125

Dual slope ADC is more accurate.

Hence (B) is correct answer.

SOL 5.126

Dual form of any identity can be find by replacing all AND function to OR and vice-versa. so here dual form will be

$$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$$

Hence (A) is correct answer.

SOL 5.127

Carry flag will be affected by arithmetic instructions only.
Hence (B) is correct answer.

SOL 5.128

This is a synchronous counter. we can find output as

Q_A	Q_B
0	0
1	0
0	1
0	0
\vdots	

So It counts only three states. It is a mod-3 counter.

$$K = 3$$

Hence (C) is correct answer.

SOL 5.129

Hence (B) is correct answer.

SOL 5.130

Essential prime implicants for a function is no. of terms that we get by solving K -map. Here we get 4 terms when solve the K -map.

AB	00	01	11	10
CD	00	01	11	10
00	1	1		1
01				1
11	1			
10	1			1

$$y = \overline{B} \overline{D} + \overline{A} \overline{C} \overline{D} + \overline{C} \overline{A} \overline{B} + \overline{C} \overline{A} \overline{B}$$

so no of prime implicants is 4

Hence (A) is correct answer.



**SOL 5.131**

Hence (A) is correct answer.

SOL 5.132

For a 2 bit multiplier

$$\begin{array}{r}
 B_1 \\
 B_0 \\
 \hline
 B_1 \\
 A_0 \\
 \hline
 A_1 B_1 \\
 A_1 B_0 \\
 \hline
 C_3
 \end{array}$$

This multiplication is identical to AND operation and then addition.
Hence (B) is correct answer.

SOL 5.133

In totem pole stage output resistance will be small so it acts like a output buffer.

Hence (C) is correct answer.

SOL 5.134

Consider high output state

$$\text{fan out} = \frac{I_{OH \max}}{I_{IH \max}} = \frac{400 \text{ mA}}{20 \text{ mA}} = 20$$

Consider low output state

$$\text{fan out} = \frac{I_{OL \max}}{I_{IL \max}} = \frac{8 \text{ mA}}{0.1 \text{ mA}} = 80$$

Thus fan out is 20

Hence (B) is correct answer.

SOL 5.135

The given gate is ex-OR so output

$$F = A\bar{B} + \bar{A}B$$

Here input $B = 0$ so,

$$F = A1 + \bar{A}0 = A$$

Hence (A) is correct answer.

SOL 5.136

EI = Enabled Interrupt flag, RST will cause an Interrupt only if we enable EI .

Hence (C) is correct answer.

SOL 5.137

Here only for the range 60 to 63 H $\overline{\text{chipselect}}$ will be 0, so peripheral will correspond in this range only $\overline{\text{chipselect}} = 1$ for rest of the given address ranges.

Hence (A) is correct answer.

SOL 5.138

By executing instructions one by one
LXI H, 8A79 H (Load HL pair by value 8A79)

$$H = 8AH \quad L = 79H$$

MOV A, L (copy contain of L to accumulator)

$$A = 79H$$

ADDH (add contain of H to accumulator)

$$A = 79H = \quad 01111001$$

$$H = 8AH = \underline{\text{add } 10001010}$$

$$= A = \quad 00000011$$

$$\text{Carry} = 1$$

DAA (Carry Flag is set, so DAA adds 6 to high order four bits)

$$01111001$$

$$\text{DAA add } 10001010$$

$$A = 00000011 = 63H$$

MOV H, A (copy contain of A to H)

$$H = 63H$$

PCHL (Load program counter by HL pair)

$$PC = 6379H$$

Hence (B) is correct answer.

SOL 5.139

Hence (C) is correct answer.

SOL 5.140

NMOS In parallel makes OR Gate & in series makes AND so here





we can have

$$F = \overline{A(B + C) + DE}$$

we took complement because there is another NMOS given above (works as an inverter)

Hence (C) is correct answer.

SOL 5.141

For a J - K flip flop we have characteristic equation as

$$Q(t+1) = J\overline{Q}(t) + \overline{K}Q(t)$$

$Q(t)$ & $Q(t+1)$ are present & next states.

In given figure $J = \overline{Q}(t)$, $K = 1$ so

$$Q(t+1) = \overline{Q}(t)\overline{Q}(t) + 0Q(t)$$

$$Q(t+1) = \overline{Q}(t) [\text{complement of previous state}]$$

we have initial input $Q(t) = 0$

so for 6 clock pulses sequence at output Q will be 010101

Hence (D) is correct answer.

SOL 5.142

Hence (C) is correct answer.

SOL 5.143

By distributive property in boolean algebra we have

$$\begin{aligned} (A + BC) &= (A + B)(A + C) \\ (A + B)(A + C) &= AA + AC + AB + BC \\ &= A(1 + C) + AB + BC \\ &= A + AB + BC \\ &= A(1 + B) + BC = A + BC \end{aligned}$$

Hence (B) is correct answer.

SOL 5.144

The current in a p n junction diode is controlled by diffusion of majority carriers while current in schottky diode dominated by the flow of majority carrier over the potential barrier at metallurgical junction. So there is no minority carrier storage in schottky diode, so switching time from forward bias to reverse bias is very short compared to p n junction diode. Hence the propagation delay will reduces.

Hence (A) is correct answer.

SOL 5.145

Hence (B) is correct answer.

SOL 5.146

The total conversion time for different type of ADC are given as—
 τ is clock period

For flash type $\Rightarrow 1\tau$

Counter type $\Rightarrow (2^n - \tau) = 4095 \mu\text{sec}$

$n = \text{no. of bits}$

Integrating type conver time $> 4095 \mu\text{sec}$

successive approximation type $n\tau = 12 \mu\text{sec}$

here $n = 12$ so

$n\tau = 12$

$12\tau = 12$

so this is succ. app. type ADC.

Hence (D) is correct answer.

SOL 5.147

LDA 2003 (Load accumulator by a value 2003 H) so here total no. of memory access will be 4.

1 = Fetching instruction

2 = Read the value from memory

1 = write value to accumulator

Hence (D) is correct answer.

SOL 5.148

Storage capacitance

$$C = \frac{i}{\left(\frac{dv}{dt}\right)} = \frac{1 \times 10^{-12}}{\left(\frac{5 - 0.5}{20 \times 10^{-3}}\right)}$$

$$= \frac{1 \times 10^{-12} \times 20 \times 10^{-3}}{4.5} = 4.4 \times 10^{-15} \text{ F}$$

Hence (D) is correct answer.

SOL 5.149

$$\text{Accuracy} \pm \frac{1}{2} \text{LSB} = T_{\text{coff}} \times \Delta T$$

$$\text{or } \frac{1}{2} \times \frac{10.24}{2^{10}} = T_{\text{coff}} \times \Delta T$$





or
$$T_{\text{coeff}} = \frac{10.24}{2 \times 1024 \times (50 - 25)^\circ\text{C}} = 200 \mu\text{V}/^\circ\text{C}$$

Hence (A) is correct answer.

SOL 5.150

$$\text{No. of chips} = \frac{26 \times 2^{10} \times 8}{2^{12} \times 4} = 13$$

Hence (D) is correct answer.

SOL 5.151

Given instruction set

1000 LXI SP 27FF

1003 CALL 1006

1006 POP H

First Instruction will initialize the SP by a value

$$27\text{FF} \quad SP \leftarrow 27\text{FF}$$

CALL 1006 will "Push PC" and Load PC by value 1006

PUSH PC will store value of PC in stack

$$PC = 1006$$

27 FF SP →	10
SP ¹ →	06

now POP H will be executed

which load HL pair by stack values

$$HL = 1006 \quad \text{and}$$

$$SP = SP' + 2$$

$$SP = SP' + 2 = SP - 2 + 2 = SP$$

$$SP = 27\text{FF}$$

Hence (C) is correct answer.

Exclusive Series By Jhunjhunwala





GATE CLOUD

By R. K . Kanodia & Ashish Murolia




GATE Cloud is an exclusive series of books which offers a completely solved question bank to GATE aspirants. The book of this series are featured as

- Over 1300 Multiple Choice Questions with full & detailed explanations.
- Questions are graded in the order of complexity from basic to advanced level.
- Contains all previous year GATE and IES exam questions from various branches
- Each question is designed to GATE exam level.
- Step by step methodology to solve problems

Available Title In this series

-  Signals and Systems (For EC and EE)
-  Network Analysis (For EC)-- Available in 2 Volumes
-  Electric Circuit and Fields (For EE) -- Available in two volumes
-  Electromagnetic (For EC)

Upcoming titles in this series

-  Digital Electronics (Nov 2012)
-  Control Systems (Dec 2012)
-  Communication Systems (Jan 2012)

For Sample chapter please mail to enquiry@nodia.co.in or visit www.nodia.co.in

Exclusive Series By Jhunjhunwala

GATE GUIDE




Theory, Example and Practice

By R. K . Kanodia & Ashish Murolia




GATE GUIDE is an exclusive series of books which provides theory, solved examples & practice exercises for preparing for GATE. A book of this series includes :

- **Brief and explicit theory**
- **Problem solving methodology**
- **Detailed explanations of examples**
- **Practice Exercises**

Available Title In this series

-  **Signals and Systems (For EC and EE)**
-  **Network Analysis (For EC)**
-  **Electric Circuit and Fields (For EE)**

Upcoming titles in this series

-  **Digital Electronics(For EC and EE)**
-  **Control Systems (For EC and EE)**
-  **Communication Systems (For EC and EE)**

For Sample chapter please mail to enquiry@nodia.co.in or visit www.nodia.co.in