# Design of Basic Computer

Introduction: Design of Basic Computer

- The basic computer consists of the following hardware components
  - 1. A memory unit with 4096 words of 16bits
  - 2. Nine registers : AR, PC, DR, AC, IR, TR, OUTR, INPR, and SC
  - 3. Seven F/Fs : I, S, E, R, IEN, FGI, and FGO
  - 4. Two decoder in control unit : 3 x 8 operation decoder, 4 x 16 timing

    decoder
  - 5. A 16-bit common bus
  - ***6. Control Logic Gates*** :
  - ***7. Adder and Logic circuit connected to the AC input***
- Control Logic Gates
  - 1. Signals to control the inputs of the nine registers
  - 2. Signals to control the read and write inputs of memory
  - 3. Signals to set, clear, or complement the F/Fs
  - 4. Signals for $S_2 S_1 S_0$ to select a register for the bus
  - 5. Signals to control the AC adder and logic circuit
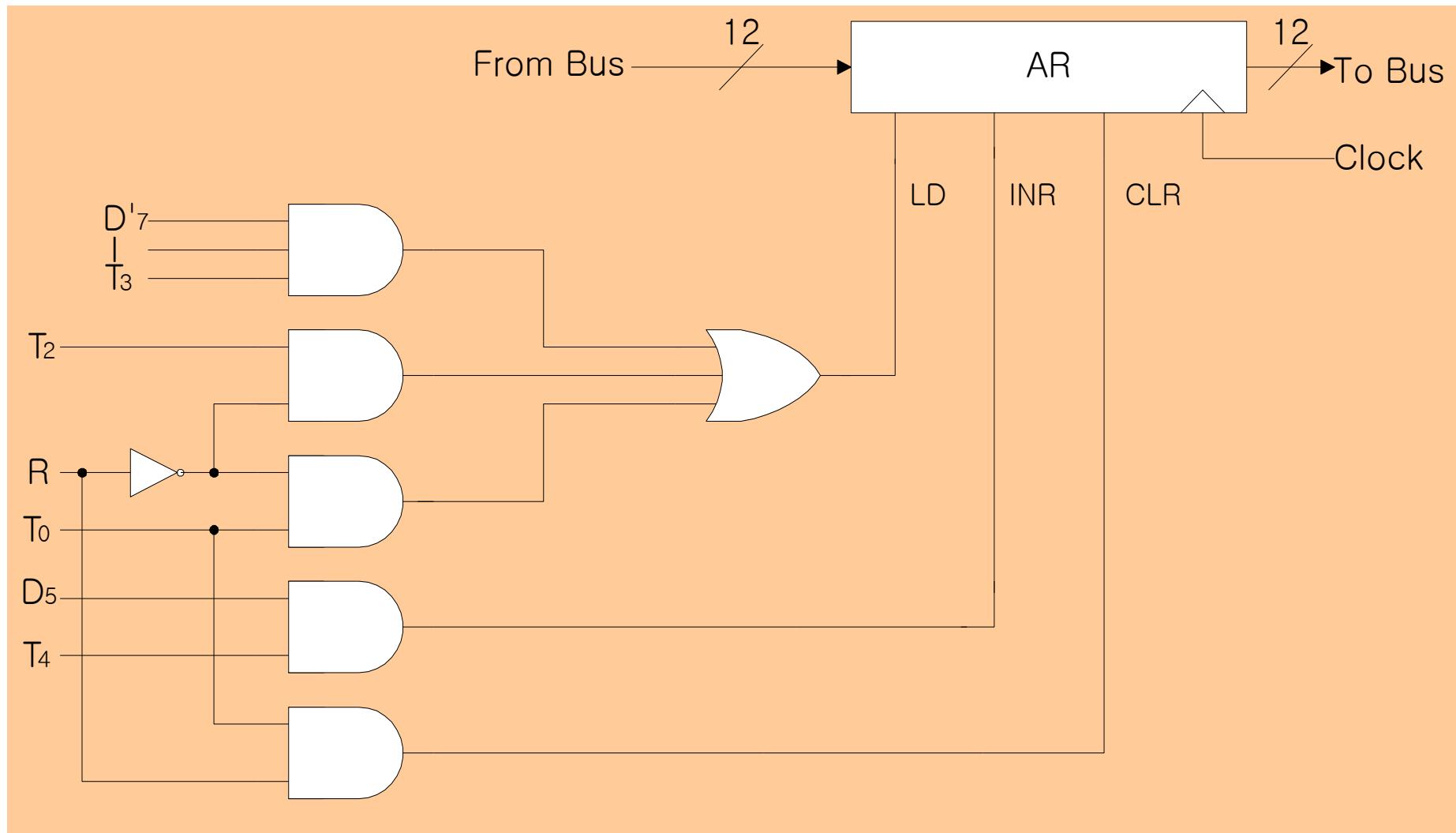
- Register Control : AR
  - Control inputs of AR : *LD, INR, CLR*
  - ***Find all the statements that change the AR in Tab. 5-6***
  - Control functions

$AR \leftarrow ?$

$$LD(AR) = R'T_0 + R'T_1 + D_7'IT_3$$
$$CLR(AR) = RT_0$$
$$INR(AR) = D_5T_4$$
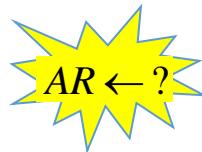
$$R'T_0 : AR \leftarrow PC$$
$$R'T_1 : AR \leftarrow IR(0-11)$$
$$D_7'IT_3 : AR \leftarrow M[AR]$$
$$RT_0 : AR \leftarrow 0$$
$$D_5T_4 : AR \leftarrow AR+1$$

- Memory Control : READ
  - Control inputs of Memory : *READ, WRITE*
  - Find all the statements that specify a *read operation* in Tab. 5-6
  - Control function

$M[AR] \leftarrow ?$

$? \leftarrow M[AR]$

$$READ = R'T_1 + D_7'IT_3 + (D_0 + D_1 + D_2 + D_3)T_4$$

- F/F Control : IEN
  - Control functions

$IEN \leftarrow ?$

$$pB_7 : IEN \leftarrow 1$$
$$pB_6 : IEN \leftarrow 0$$
$$RT_2 : IEN \leftarrow 0$$

J	K	Q(t+1)
0	1	0
1	0	1

- Bus Control
  - Encoder for Bus Selection : *Tab. 5-7*
    - $S_0 = x_1 + x_3 + x_5 + x_7$
    - $S_1 = x_2 + x_3 + x_6 + x_7$ $Bus \leftarrow AR = Find\ ? \leftarrow AR$
    - $S_0 = x_4 + x_5 + x_5 + x_7$
  - $x_1 = 1$:
    - $D_4T_4 : PC \leftarrow AR$

    $D_5T_5 : PC \leftarrow AR$

    - Control Function : $x_1 = D_4T_4 + D_5T_5$
  - $x_2 = 1$:

    $Bus \leftarrow PC = Find\ ? \leftarrow PC$

    "
  - $x_7 = 1$: "
    - Same as Memory Read
    - Control Function : $Bus \leftarrow Memory = Find\ ? \leftarrow M[AR]$

x_1
x_2
x_3
x_4
x_5
x_6
x_7

Encoder

SMultiplexer
SBus Select
SInput

$x_7 = R'T_1 + D_7'IT_3 + (D_0 + D_1 + D_2 + D_3)T_4$
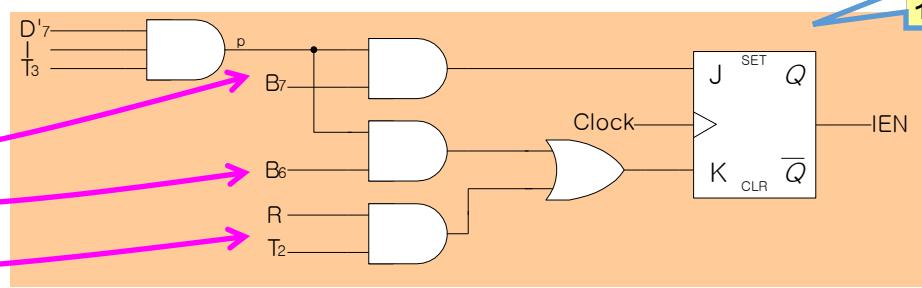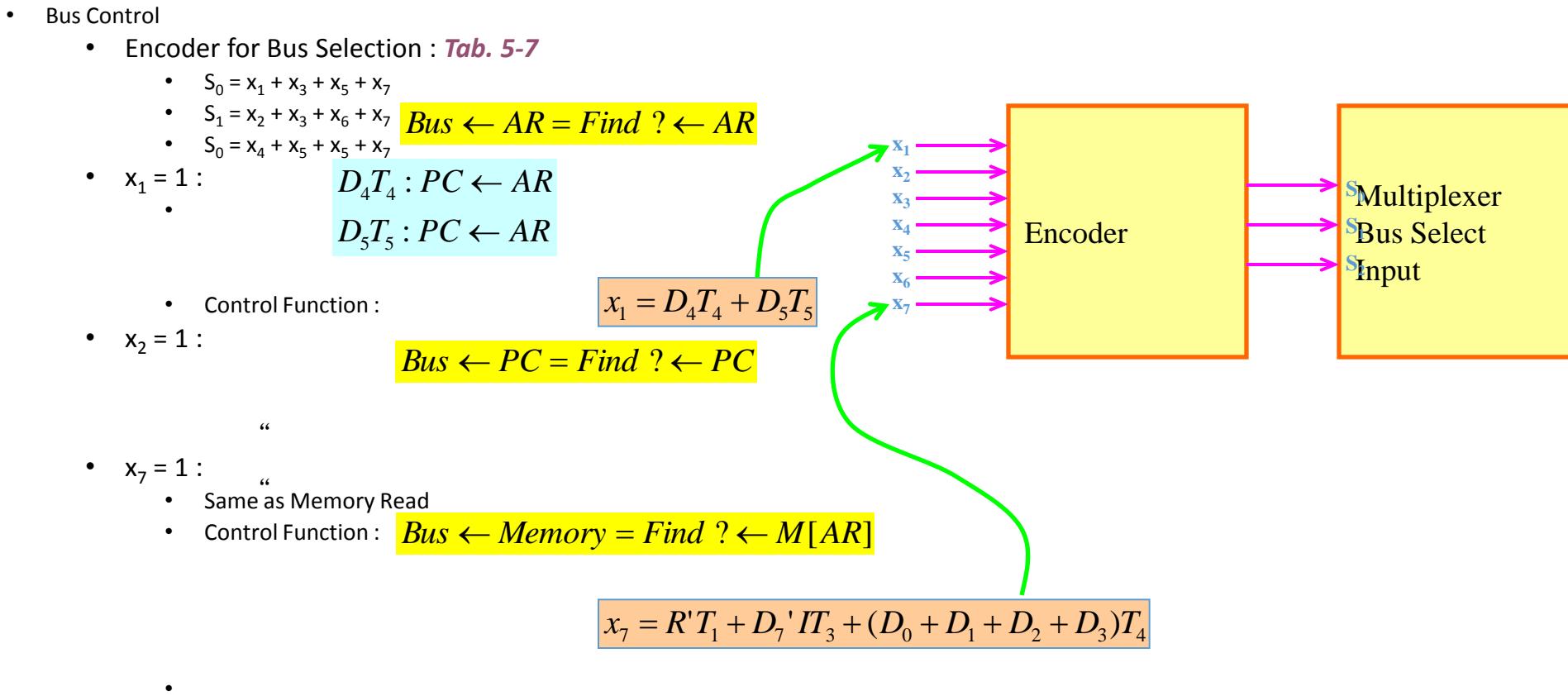
- Design of Accumulator Logic
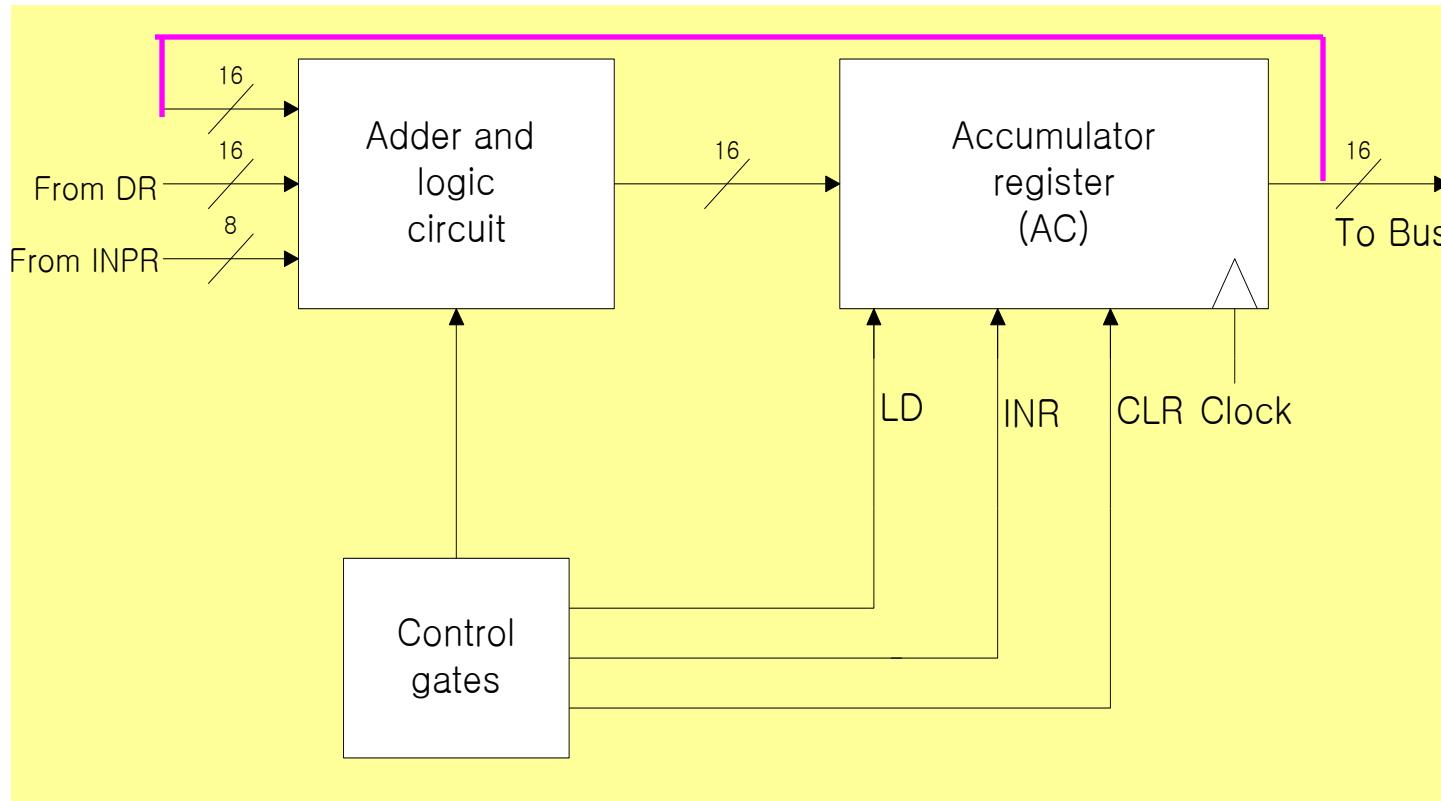
Circuits associated with Accumulator

Memory reference
- AND with DR
- ADD with DR
- Transfer from DR

I/O reference
- Transfer from INPR

Register reference
- Complement
- Shift right
- Shift left
- Clear
- Increment

$$D_0 T_5 : AC \leftarrow AC \wedge DR$$

$$D_1 T_5 : AC \leftarrow AC + DR$$

$$D_2 T_5 : AC \leftarrow DR$$

$$pB_{11} : AC(0-7) \leftarrow INPR$$

$$rB_9 : AC \leftarrow \overline{AC}$$

$$rB_7 : AC \leftarrow shr\ AC,\ AC(15) \leftarrow E$$

$$rB_6 : AC \leftarrow shl\ AC,\ AC(0) \leftarrow E$$

$$rB_{11} : AC \leftarrow 0$$

$$rB_5 : AC \leftarrow AC + 1$$

LD

CLR

INR
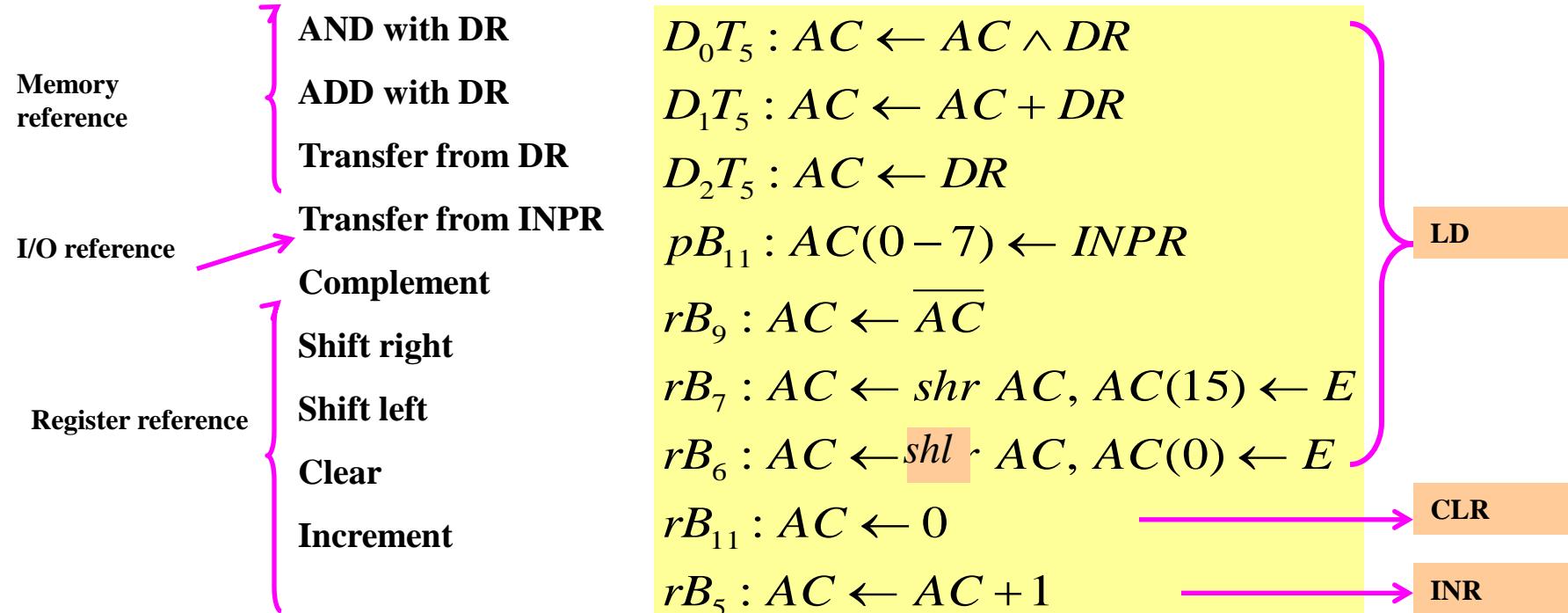
Gate Structure for Controlling LD, INR, CLR & AC
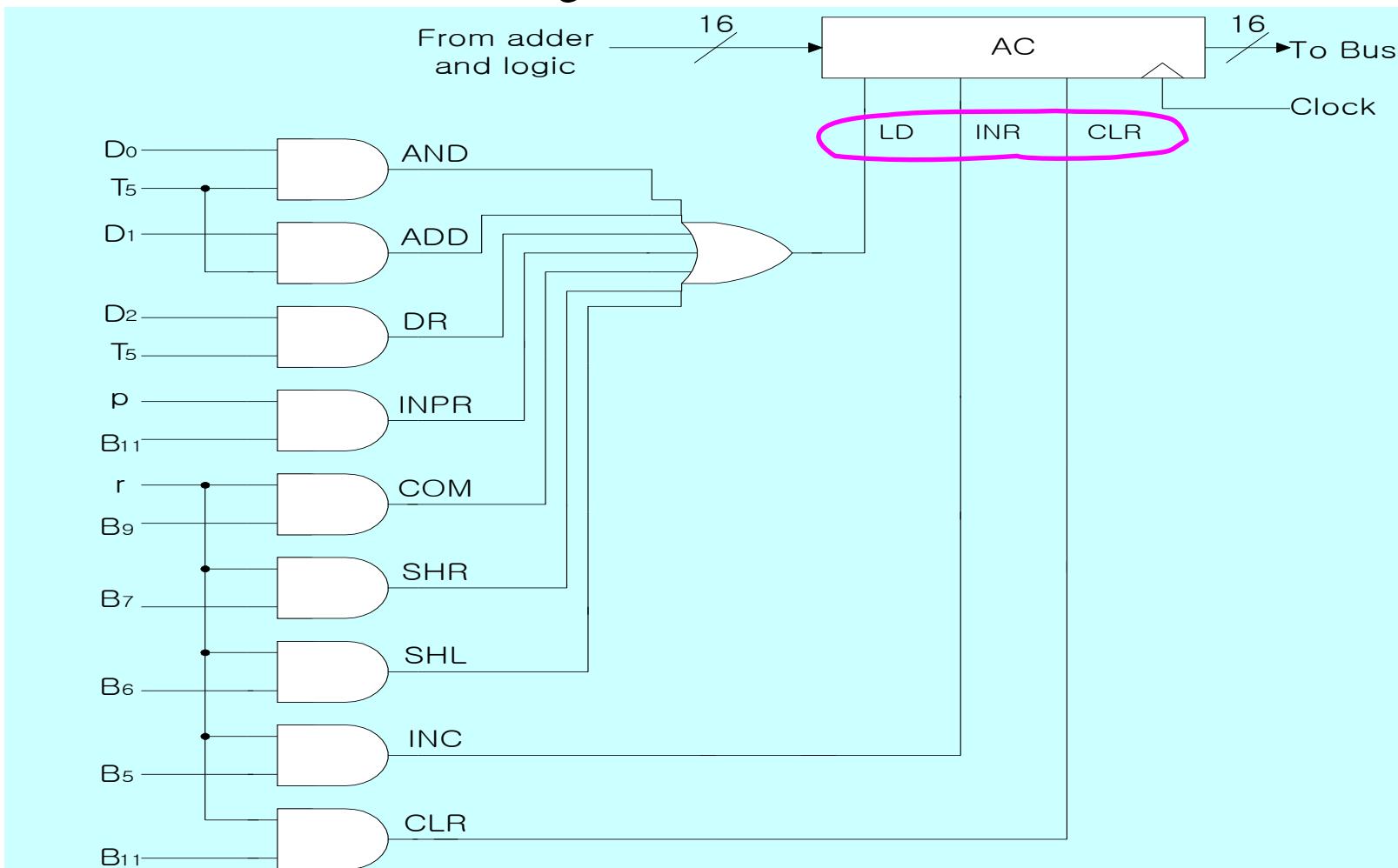
The control function for the clear operation is rB11 where r=D7I'T3 AND B11 =IR(11).

- Adder and Logic Circuit : *The adder and logic circuit is devided into 16 stages with each stage corresponding to one bit of AC.*

- *Each stage has a JK flip flop, 2 OR gate , and two AND gate.*

- *The LD input is connected to the input of AND Gate.*

- *Note: one stage of Adder and logic ckt consist of seven AND Gate, One OR Gate and a FULL ADDER(FA).*

- *The AND operation is achieved with ANDing AC(i) with the corresponding bit in the DR(i).*

DR(i) AC(i)

(Output of OR gate in Fig. 5-20)

AND
ADD
C_i
FA
C_{i+1}
DR
INPR
From INPR bit(i)
COM
SHR
AC(i+1)
SHL
AC(i-1)

I_i (Fig.2-11)

LD
J Q AC(i)
K
Clock

J	K	Q(t+1)
0	1	0
1	0	1
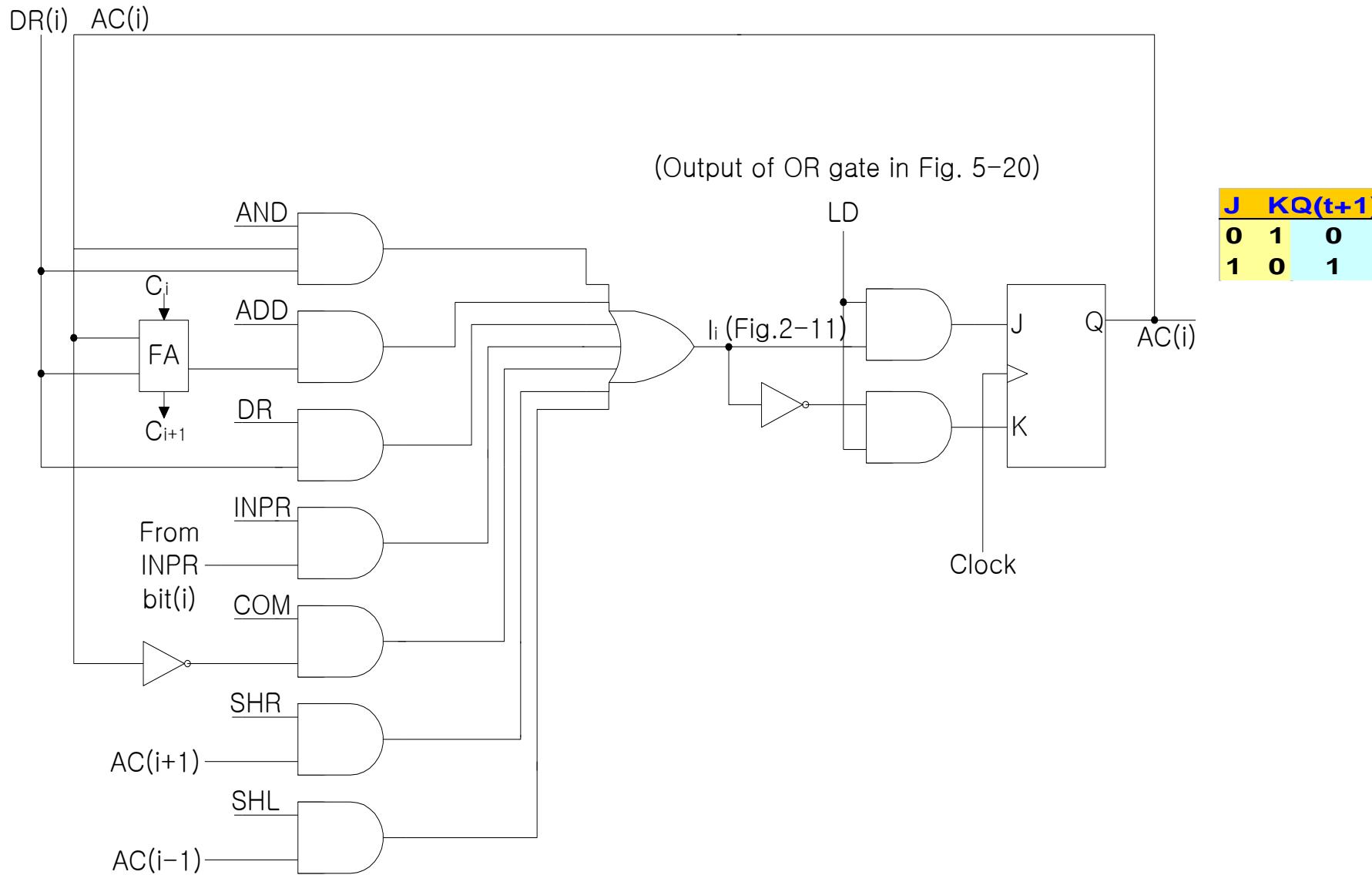
Assignment

Design accumulator with the help of GATES.